DATA SHEET

NE5517/NE5517A
Dual operational transconductance amplifier

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Philips Semiconductors

PHILIPS

Dual operational transconductance amplifier NE5517/NE5517A

DESCRIPTION

The NE5517 contains two current-controlled transconductance amplifiers, each with a differential input and push-pull output. The NE5517 offers significant design and performance advantages over similar devices for all types of programmable gain applications. Circuit performance is enhanced through the use of linearizing diodes at the inputs which enable a 10 dB signal-to-noise improvement referenced to 0.5% THD. The NE5517 is suited for a wide variety of industrial and consumer applications and is recommended as the preferred circuit in the Dolby™ HX (Headroom Extension) system.

Constant impedance buffers on the chip allow general use of the NE5517. These buffers are made of Darlington transistor and a biasing network which changes bias current in dependence of I_{ABC}.

Therefore, changes of output offset voltages are almost eliminated. This is an advantage of the NE5517 compared to LM13600. With the LM13600, a burst in the bias current I_{ABC} guides to an audible offset voltage change at the output. With the constant impedance buffers of the NE5517 this effect can be avoided and makes this circuit preferable for high quality audio applications.

FEATURES

- Constant impedance buffers
- ΔV_{BE} of buffer is constant with amplifier I_{BIAS} change
- Pin compatible with LM13600
- Excellent matching between amplifiers
- Linearizing diodes
- High output signal-to-noise ratio

APPLICATIONS

- Multiplexers
- Timers
- Electronic music synthesizers
- Dolby™ HX Systems
- Current-controlled amplifiers, filters
- Current-controlled oscillators, impedances

PIN CONFIGURATION

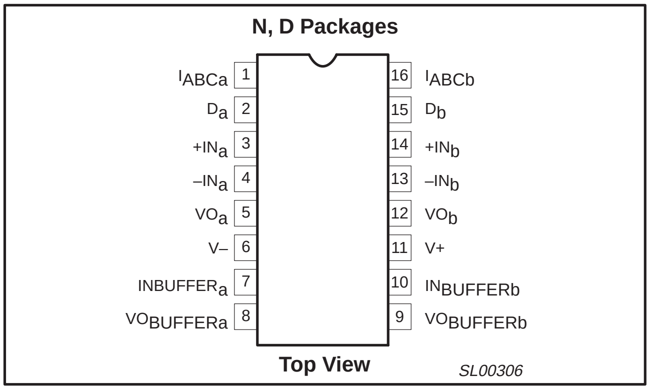

Figure 1. Pin Configuration

PIN DESIGNATION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	I_{ABCa}	Amplifier bias input A
2	D_a	Diode bias A
3	$+IN_a$	Non-inverting input A
4	$-IN_a$	Inverting input A
5	V_{Oa}	Output A
6	V–	Negative supply
7	$IN_{BUFFERa}$	Buffer input A
8	$VO_{BUFFERa}$	Buffer output A
9	$VO_{BUFFERb}$	Buffer output B
10	$IN_{BUFFERb}$	Buffer input B
11	V+	Positive supply
12	V_{Ob}	Output B
13	$-IN_b$	Inverting input B
14	$+IN_b$	Non-inverting input B
15	D_b	Diode bias B
16	I_{ABCb}	Amplifier bias input B

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Dual In-Line Package (DIP)	0 to +70 °C	NE5517N	SOT38-4
16-Pin Plastic Dual In-Line Package (DIP)	0 to +70 °C	NE5517AN	SOT38-4
16-Pin Small Outline (SO) Package	0 to +70 °C	NE5517D	SOT109-1

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CIRCUIT SCHEMATIC

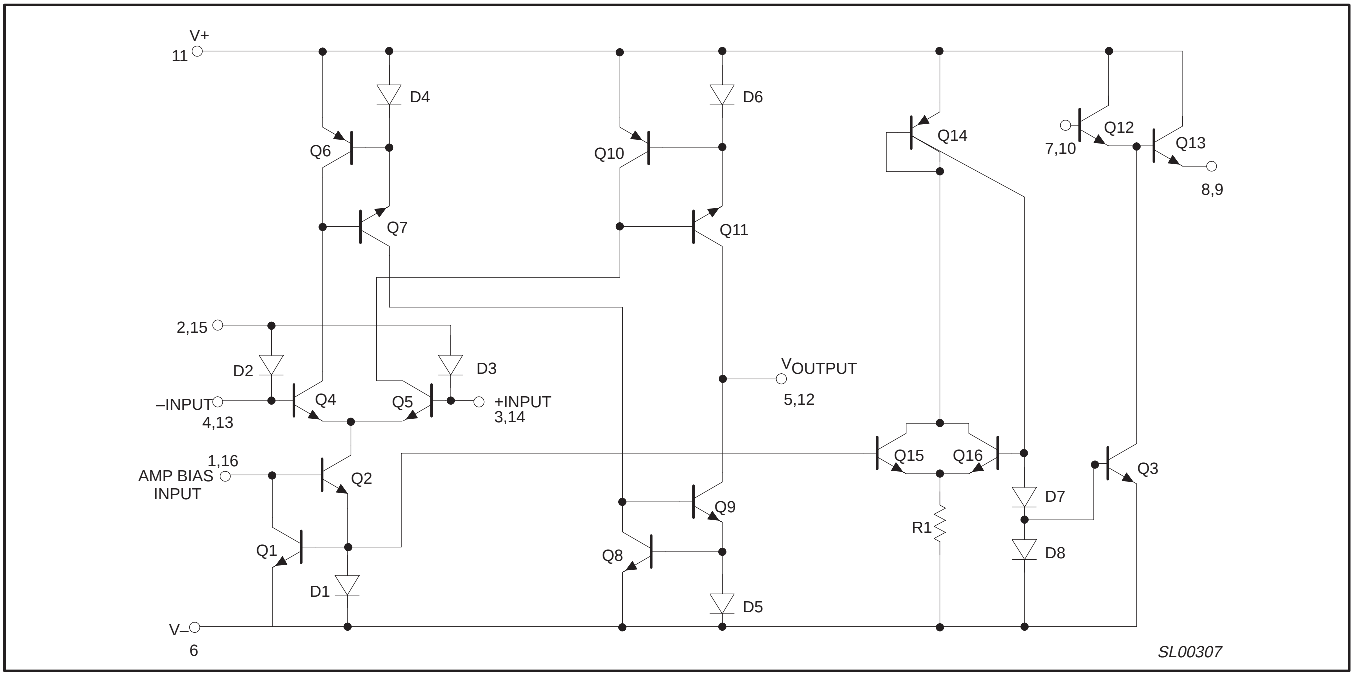
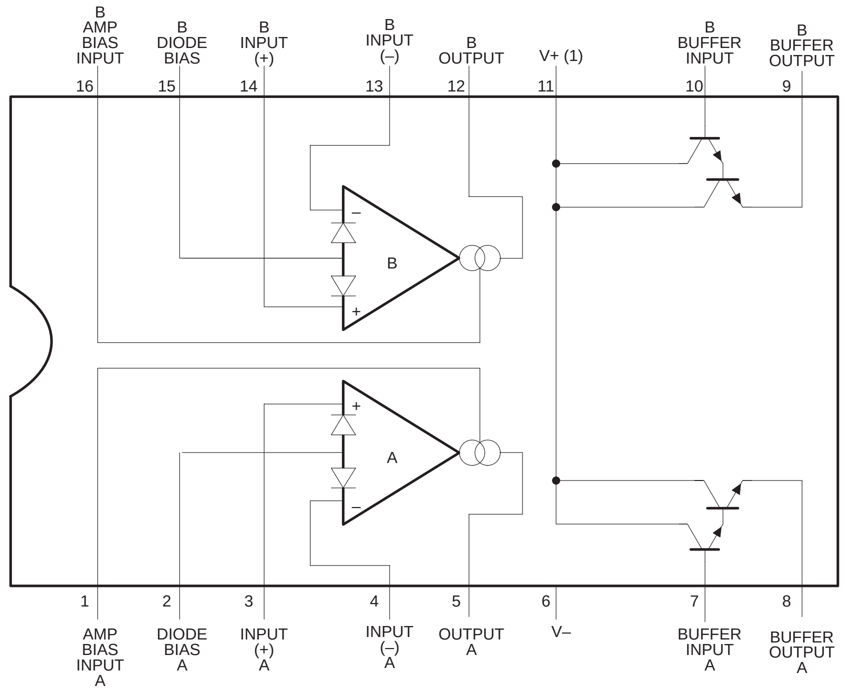


Figure 2. Circuit Schematic

CONNECTION DIAGRAM



NOTE:
1. V+ of output buffers and amplifiers are internally connected.

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Figure 3. Connection Diagram

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_S	Supply voltage[1] NE5517 NE5517A	 36 V_{DC} or ±18 44 V_{DC} or ±22	 V V
P_D	Power dissipation, T_{amb} = 25 °C (still air)[2] NE5517N, NE5517AN NE5517D	 1500 1125	 mW mW
V_{IN}	Differential input voltage	±5	V
I_D	Diode bias current	2	mA
I_{ABC}	Amplifier bias current	2	mA
I_{SC}	Output short-circuit duration	Indefinite	
I_{OUT}	Buffer output current[3]	20	mA
T_{amb}	Operating temperature range NE5517N, NE5517AN	 0 °C to +70 °C	 °C
V_{DC}	DC input voltage	$+V_S$ to $-V_S$	
T_{stg}	Storage temperature range	–65 °C to +150 °C	°C
T_{sld}	Lead soldering temperature (10 sec max)	230	°C

NOTES:
1. For selections to a supply voltage above ±22 V, contact factory
2. The following derating factors should be applied above 25 °C
   N package at 12.0 mW/°C
   D package at 9.0 mW/°C
3. Buffer output current should be limited so as to not exceed package dissipation.

DC ELECTRICAL CHARACTERISTICS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	NE5517			NE5517A			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage	 Over temperature range I_{ABC} 5 µA		0.4 0.3	5 5		0.4 0.3	2 5 2	mV mV mV
	$\Delta V_{OS}/\Delta T$	Avg. TC of input offset voltage		7			7		µV/°C
	V_{OS} including diodes	Diode bias current (I_D) = 500 µA		0.5	5		0.5	2	mV
V_{OS}	Input offset change	5 µA ≤ I_{ABC} ≤ 500 µA		0.1			0.1	3	mV
I_{OS}	Input offset current			0.1	0.6		0.1	0.6	µA
	$\Delta I_{OS}/\Delta T$	Avg. TC of input offset current		0.001			0.001		µA/°C
I_{BIAS}	Input bias current	 Over temperature range		0.4 1	5 8		0.4 1	5 7	µA µA
	$\Delta I_B/\Delta T$	Avg. TC of input current		0.01			0.01		µA/°C
g_M	Forward transconductance	 Over temperature range	6700 5400	9600	1300	7700 4000	9600	1200	µmho µmho
	g_M tracking			0.3			0.3		dB
I_{OUT}	Peak output current	R_L = 0, I_{ABC} =5 µA R_L = 0, I_{ABC} = 500 µA R_L = 0	 350 300	5 500	 650	3 350 300	5 500	7 650	µA µA µA
V_{OUT}	Peak output voltage Positive Negative	 R_L = ∞, 5 µA ≤ I_{ABC} ≤ 500 µA R_L = ∞, 5 µA ≤ I_{ABC} ≤ 500 µA	 +12 –12	 +14.2 –14.4		 +12 –12	 +14.2 –14.4		 V V
I_{CC}	Supply current	I_{ABC} = 500 µA, both channels		2.6	4		2.6	4	mA
	V_{OS} sensitivity Positive Negative	 Δ V_{OS}/Δ V+ Δ V_{OS}/Δ V–		 20 20	 150 150		 20 20	 150 150	 µV/V µV/V
CMRR	Common-mode rejection ration		80	110		80	110		dB
	Common-mode range		±12	±13.5		±12	±13.5		V
	Crosstalk	Referred to input[2] 20 Hz < f < 20 kHz		100			100		dB
I_{IN}	Differential input current	I_{ABC} = 0, input = ±4 V		0.02	100		0.02	10	nA
	Leakage current	I_{ABC} = 0 (Refer to test circuit)		0.2	100		0.2	5	nA
R_{IN}	Input resistance		10	26		10	26		kΩ
B_W	Open-loop bandwidth			2			2		MHz
SR	Slew rate	Unity gain compensated		50			50		V/µs
IN_{BUFFER}	Buffer input current	5		0.4	5		0.4	5	µA
VO_{BUFFER}	Peak buffer output voltage	5	10			10			V
	ΔV_{BE} of buffer	Refer to Buffer V_{BE} test circuit [3]		0.5	5		0.5	5	mV

NOTES:
1. These specifications apply for V_S = ±15 V, T_{amb} = 25 °C, amplifier bias current (I_{ABC}) = 500 µA, Pins 2 and 15 open unless otherwise specified. The inputs to the buffers are grounded and outputs are open.
2. These specifications apply for V_S = ±15 V, I_{ABC} = 500 µA, R_{OUT} = 5 kΩ connected from the buffer output to $–V_S$ and the input of the buffer is connected to the transconductance amplifier output.
3. V_S = ±15, R_{OUT} = 5 kΩ connected from Buffer output to $–V_S$ and 5 µA ≤ I_{ABC} ≤ 500 µA.

TYPICAL PERFORMANCE CHARACTERISTICS

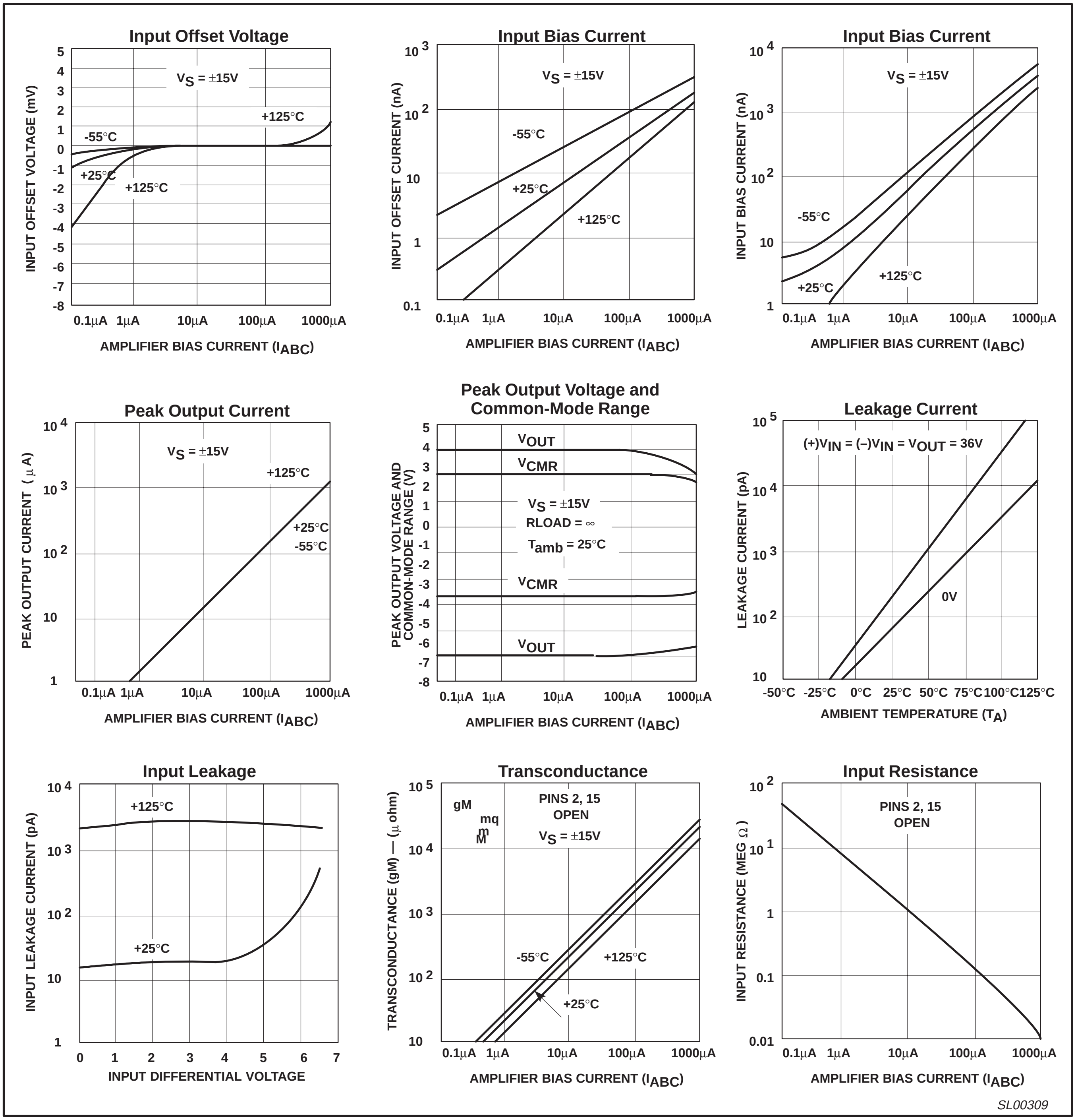


Figure 4. Typical Performance Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

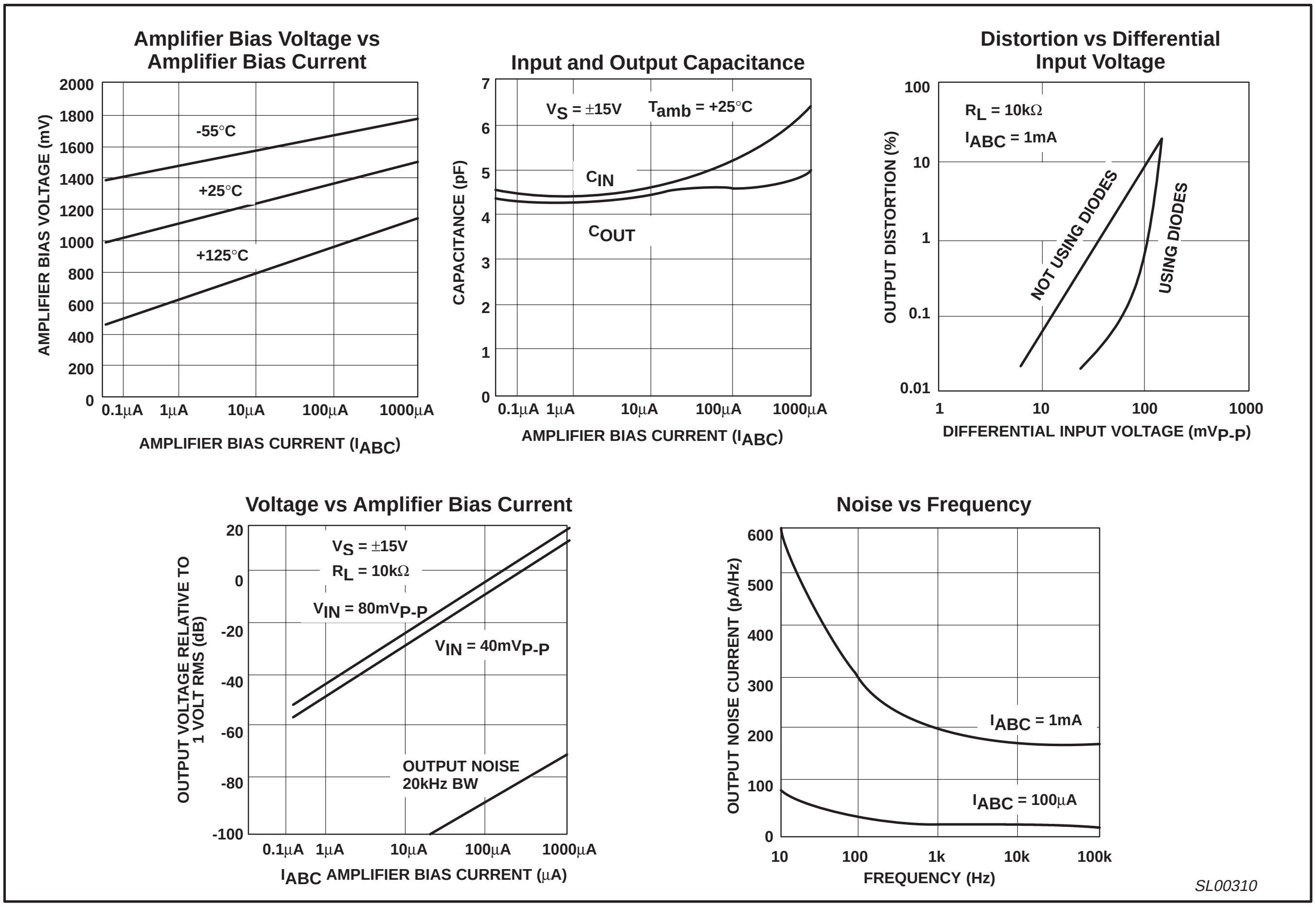
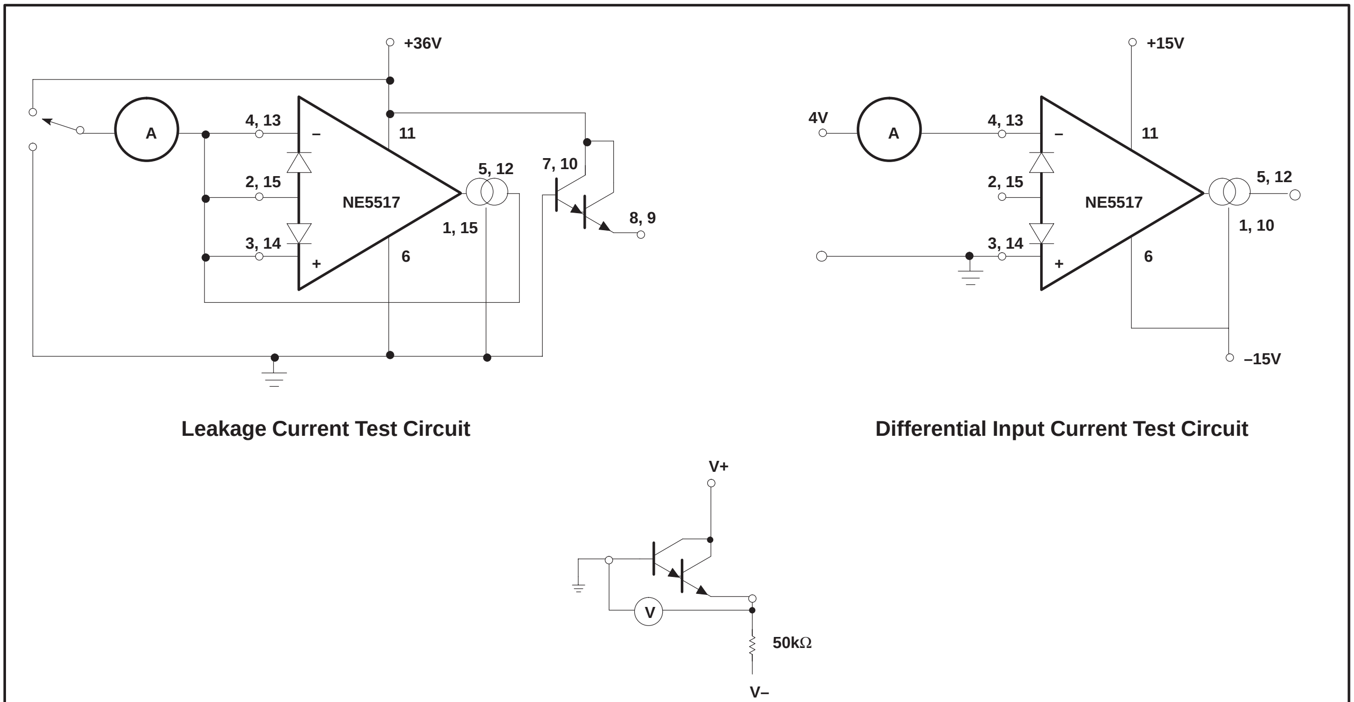


Figure 5. Typical Performance Characteristics (cont.)

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



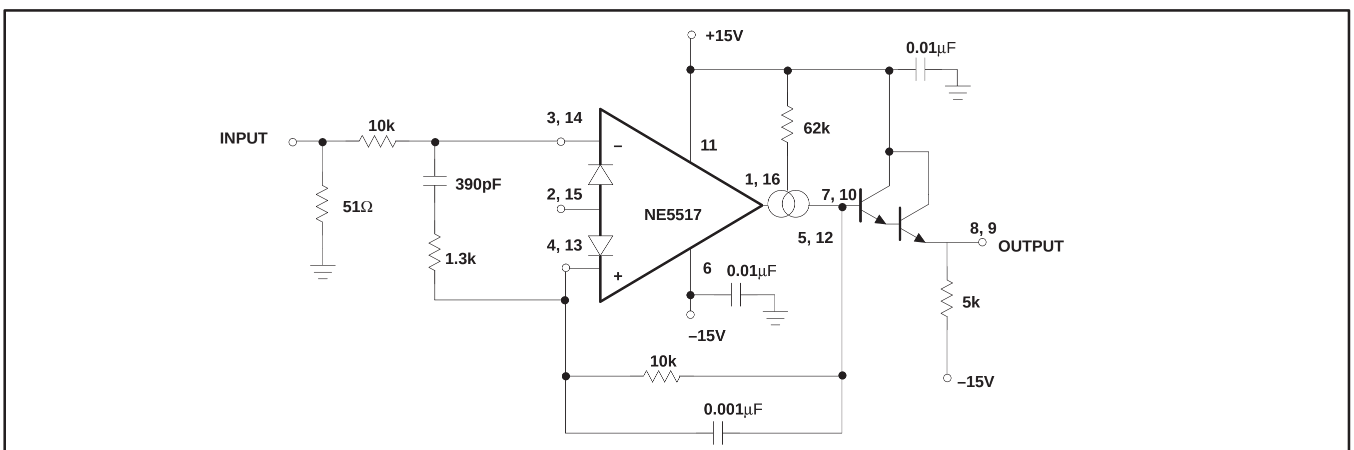
Leakage Current Test Circuit

Differential Input Current Test Circuit

Buffer V_{BE} Test Circuit

Figure 6. Typical Performance Characteristics (cont.)

APPLICATIONS



Unity Gain Follower

Figure 7. Applications

CIRCUIT DESCRIPTION

The circuit schematic diagram of one-half of the NE5517, a dual operational transconductance amplifier with linearizing diodes and impedance buffers, is shown in Figure 8.

1. Transconductance Amplifier

The transistor pair, Q_4 and Q_5, forms a transconductance stage. The ratio of their collector currents (I_4 and I_5, respectively) is defined by the differential input voltage, V_{IN}, which is shown in equation 1.

$$V_{IN} = \frac{KT}{q} \ln \frac{I_5}{I_4} \quad (1)$$

Where V_{IN} is the difference of the two input voltages

KT ≅ 26 mV at room temperature (300 °k).

Transistors Q_1, Q_2 and diode D_1 form a current mirror which focuses the sum of current I_4 and I_5 to be equal to amplifier bias current I_B:

$$I_4 + I_5 = I_B \quad (2)$$

If V_{IN} is small, the ratio of I_5 and I_4 will approach unity and the Taylor series of In function can be approximated as

$$\frac{KT}{q} \ln \frac{I_5}{I_4} \approx \frac{KT}{q} \frac{I_5 - I_4}{I_4} \quad (3)$$

and $I_4 \cong I_5 \cong I_B$

$$\frac{KT}{q} \ln \frac{I_5}{I_4} \approx \frac{KT}{q} \frac{I_5 - I_4}{1/2 I_B} = \frac{2KT}{q} \frac{I_5 - I_4}{I_B} = V_{IN} \quad (4)$$

$$I_5 - I_4 = V_{IN} \frac{\left(I_B{}^q\right)}{2KT}$$

The remaining transistors (Q_6 to Q_{11}) and diodes (D_4 to D_6) form three current mirrors that produce an output current equal to I_5 minus I_4. Thus:

$$V_{IN}\left(I_B \frac{q}{2KT}\right) = I_O \quad (5)$$

The term $\frac{\left(I_B{}^q\right)}{2KT}$ is then the transconductance of the amplifier and is proportional to I_B.

2. Linearizing Diodes

For V_{IN} greater than a few millivolts, equation 3 becomes invalid and the transconductance increases non-linearly. Figure 9 shows how the internal diodes can linearize the transfer function of the operational amplifier. Assume D_2 and D_3 are biased with current sources and the input signal current is I_S. Since

$I_4 + I_5 = I_B$ and $I_5 – I_4 = I_0$, that is:

$I_4 = (I_B – I_0)$, $I_5 = (I_B + I_0)$

For the diodes and the input transistors that have identical geometries and are subject to similar voltages and temperatures, the following equation is true:

$$\frac{T}{q} \ln \frac{\frac{I_D}{2} + I_S}{\frac{I_D}{2} - I_S} = \frac{KT}{q} \ln \frac{1/2(I_B + I_O)}{1/2(I_B - I_O)} \quad (6)$$

$$I_O = I_S \frac{2^I B}{I_D} \text{ for } |I_S| < \frac{I_D}{2}$$

The only limitation is that the signal current should not exceed I_D.

3. Impedance Buffer

The upper limit of transconductance is defined by the maximum value of I_B (2 mA). The lowest value of I_B for which the amplifier will function therefore determines the overall dynamic range. At low values of I_B, a buffer with very low input bias current is desired. A Darlington amplifier with constant-current source (Q_{14}, Q_{15}, Q_{16}, D_7, D_8, and R_1) suits the need.

APPLICATIONS

Voltage-Controlled Amplifier

In Figure 10, the voltage divider R_2, R_3 divides the input-voltage into small values (mV range) so the amplifier operates in a linear manner.

It is:

$$I_{OUT} = -V_{IN} \cdot \frac{R_3}{R_2 + R_3} \cdot gM;$$

$$V_{OUT} = I_{OUT} \cdot R_L;$$

$$\boxed{A = \frac{V_{OUT}}{V_{IN}} = \frac{R_3}{R_2 + R_3} \cdot gM \cdot R_L}$$

(3) $g_M = 19.2\ I_{ABC}$

(g_M in µmhos for I_{ABC} in mA)

Since g_M is directly proportional to I_{ABC}, the amplification is controlled by the voltage V_C in a simple way.

When V_C is taken relative to $–V_{CC}$ the following formula is valid:

$$I_{ABC} = \frac{(V_C - 1.2V)}{R_1}$$

The 1.2 V is the voltage across two base-emitter baths in the current mirrors. This circuit is the base for many applications of the NE5517.

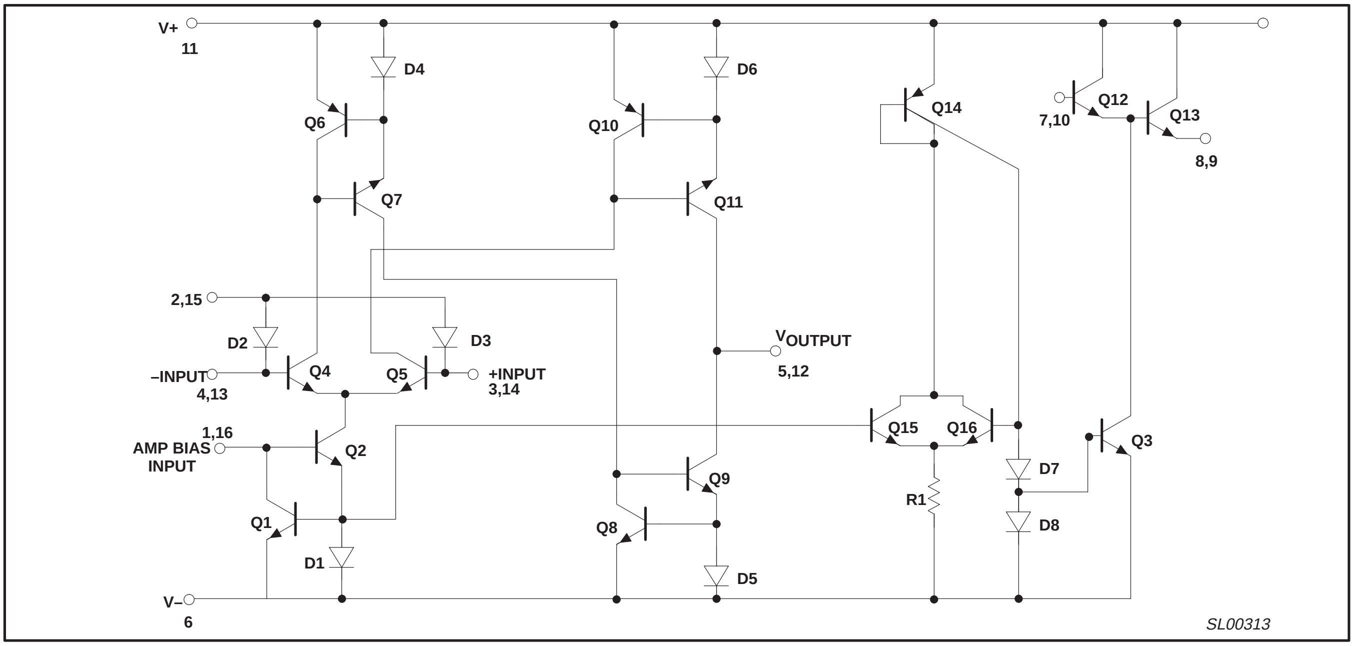


Figure 8. Circuit Diagram of NE5517

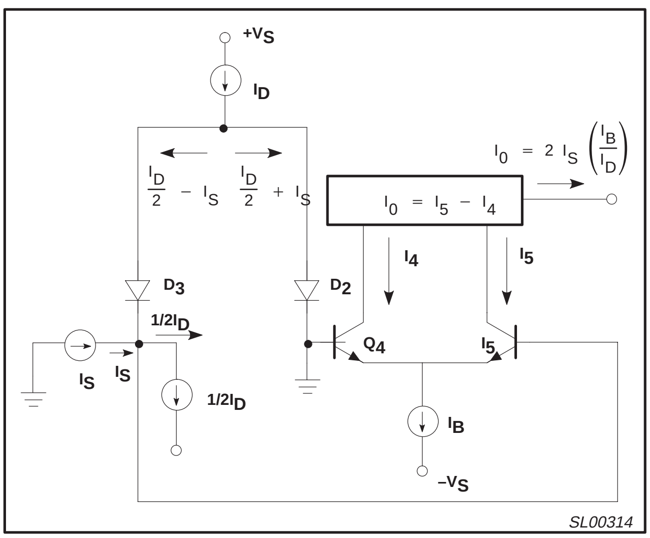


Figure 9. Linearizing Diode

Stereo Amplifier With Gain Control

Figure 11 shows a stereo amplifier with variable gain via a control input. Excellent tracking of typical 0.3 dB is easy to achieve. With the potentiometer, R_P, the offset can be adjusted. For AC-coupled amplifiers, the potentiometer may be replaced with two 510 Ω resistors.

Modulators

Because the transconductance of an OTA (Operational Transconductance Amplifier) is directly proportional to I_{ABC}, the amplification of a signal can be controlled easily. The output current is the product from transconductance×input voltage. The circuit is effective up to approximately 200 kHz. Modulation of 99% is easy to achieve.

Voltage-Controlled Resistor (VCR)

Because an OTA is capable of producing an output current proportional to the input voltage, a voltage variable resistor can be made. Figure 13 shows how this is done. A voltage presented at the R_X terminals forces a voltage at the input. This voltage is multiplied by g_M and thereby forces a current through the R_X terminals:

$$R_X = \frac{R + R_A}{gM + R_A}$$

where g_M is approximately 19.21 μMHOs at room temperature. Figure 14 shows a Voltage Controlled Resistor using linearizing diodes. This improves the noise performance of the resistor.

Voltage-Controlled Filters

Figure 15 shows a Voltage Controlled Low-Pass Filter. The circuit is a unity gain buffer until X_C/g_M is equal to R/R_A. Then, the frequency response rolls off at a 6dB per octave with the –3 dB point being defined by the given equations. Operating in the same manner, a Voltage Controlled High-Pass Filter is shown in Figure 16. Higher order filters can be made using additional amplifiers as shown in Figures 17 and 18.

Voltage-Controlled Oscillators

Figure 19 shows a voltage-controlled triangle-square wave generator. With the indicated values a range from 2 Hz to 200 kHz is possible by varying I_{ABC} from 1 mA to 10 μA.

The output amplitude is determined by $I_{OUT} \times R_{OUT}$.

Please notice the differential input voltage is not allowed to be above 5 V.

With a slight modification of this circuit you can get the sawtooth pulse generator, as shown in Figure 20.

APPLICATION HINTS

To hold the transconductance g_M within the linear range, I_{ABC} should be chosen not greater than 1 mA. The current mirror ratio should be as accurate as possible over the entire current range. A current mirror with only two transistors is not recommended. A suitable current mirror can be built with a PNP transistor array which causes excellent matching and thermal coupling among the transistors. The output current range of the DAC normally reaches from 0 to –2 mA. In this application, however, the current range is set through R_{REF} (10 kΩ) to 0 to –1 mA.

$$I_{DACMAX} = 2 \cdot \frac{V_{REF}}{R_{REF}} = 2 \cdot \frac{5V}{10k\Omega} = 1mA$$

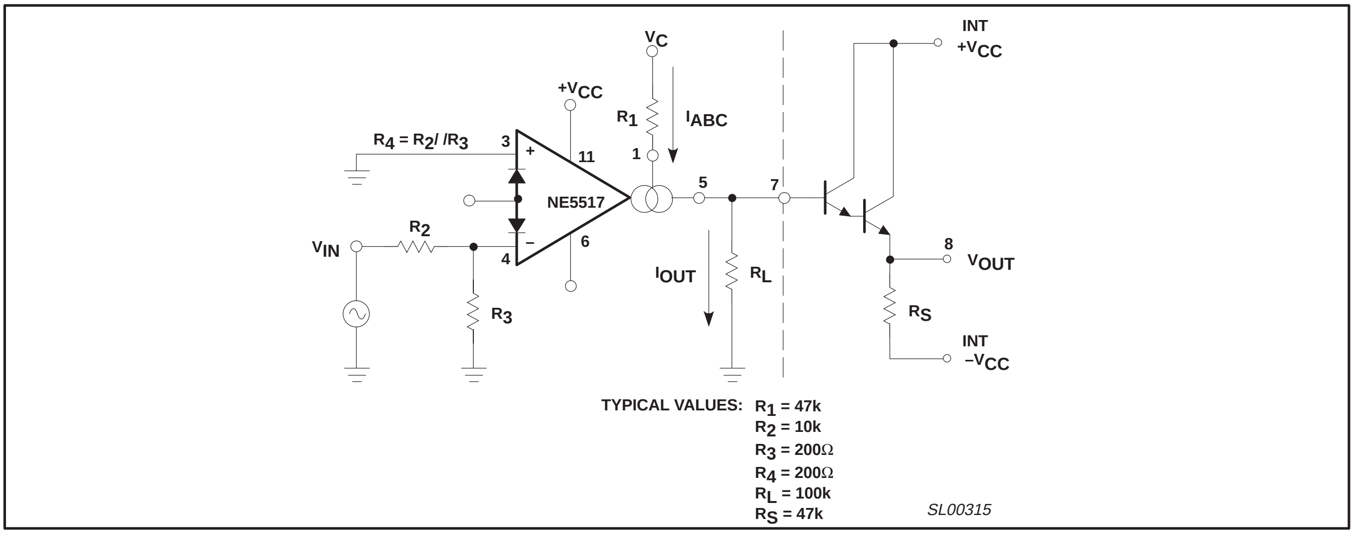


Figure 10.

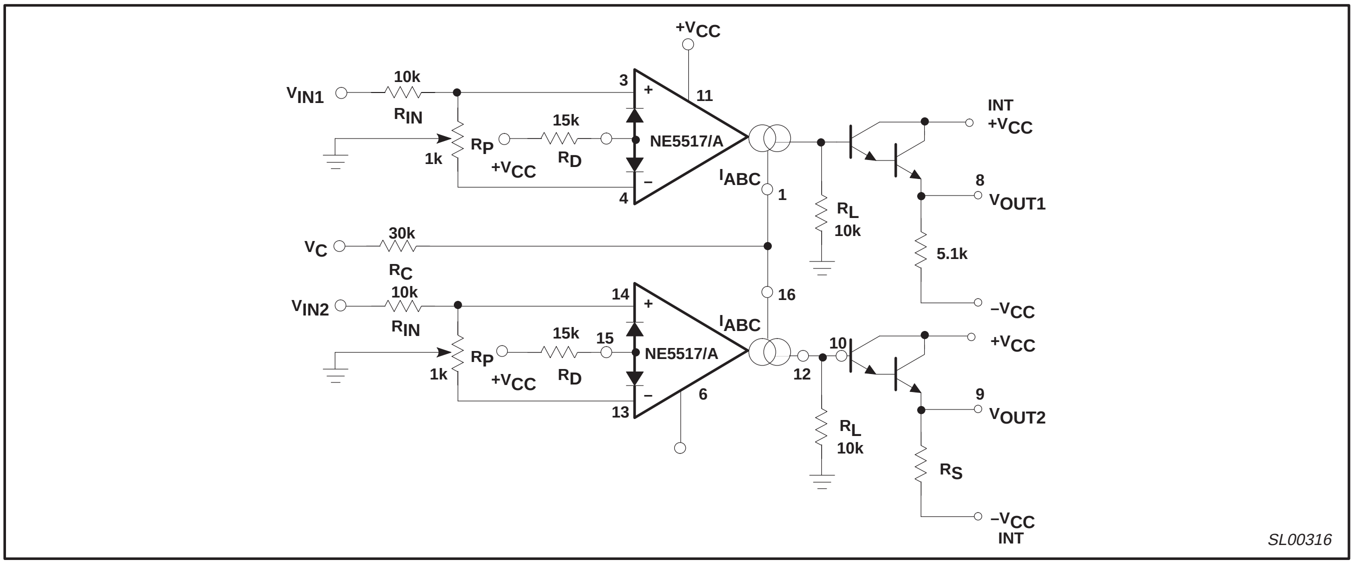


Figure 11. Gain-Controlled Stereo Amplifier

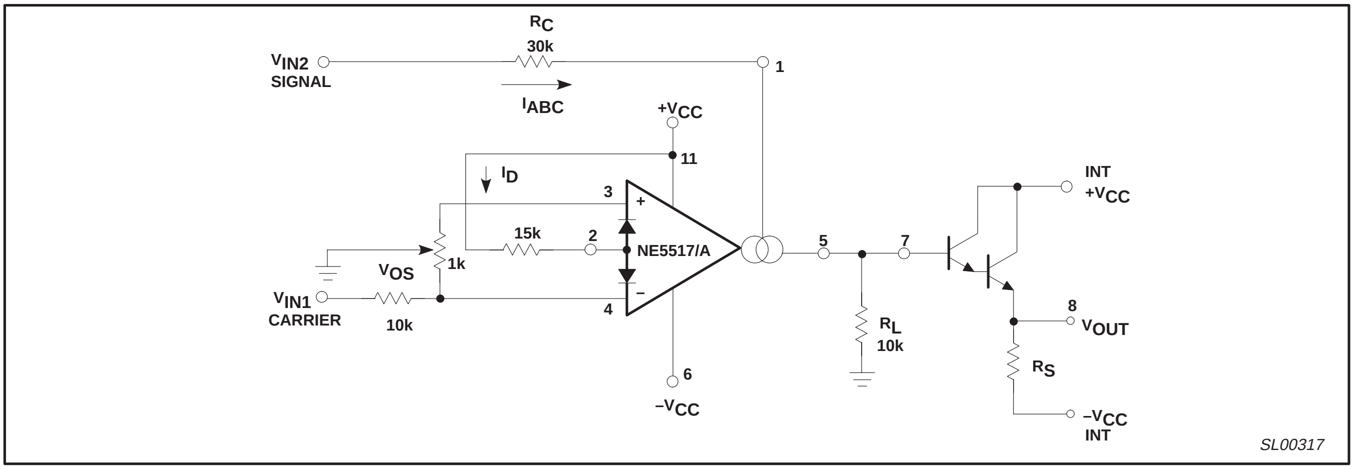


Figure 12. Amplitude Modulator

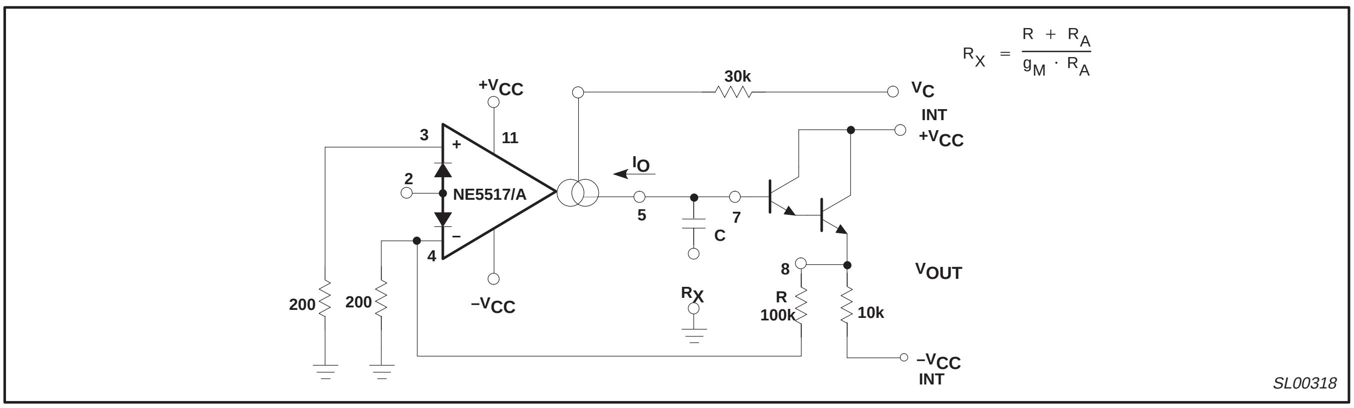


Figure 13. VCR

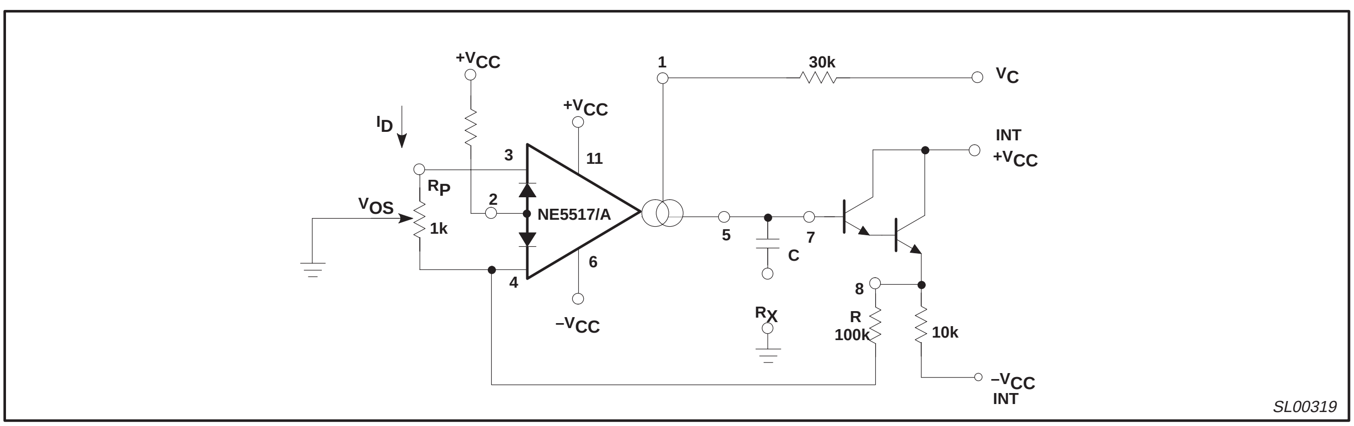
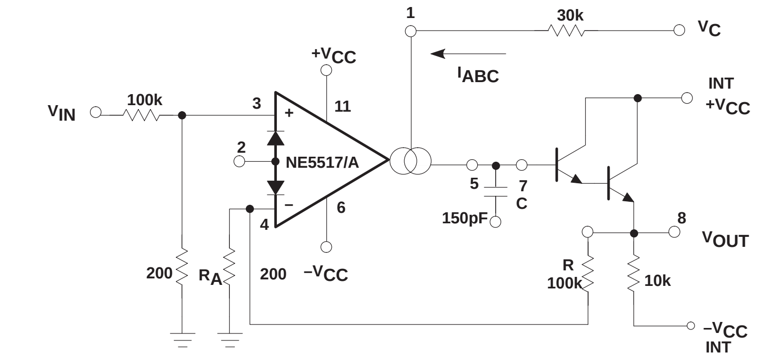


Figure 14. VCR with Linearizing Diodes



NOTE:

$$f_O = \frac{R_A\ g_M}{g(R + RA)\ 2\pi C}$$

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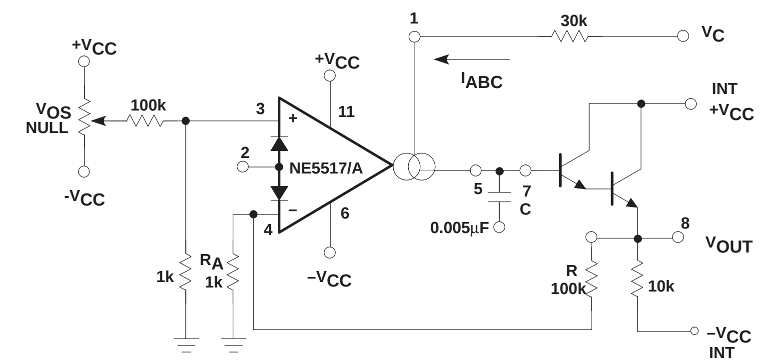
Figure 15. Voltage-Controlled Low-Pass Filter



NOTE:

$$f_O = \frac{R_A\ g_M}{g(R + RA)\ 2\pi C}$$

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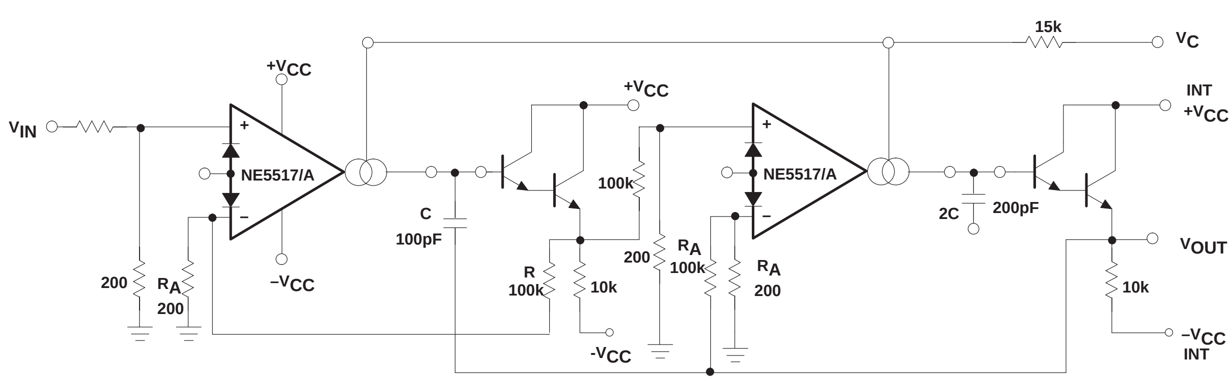
Figure 16. Voltage-Controlled High-Pass Filter



NOTE:

$$f_O = \frac{R_A\ g_M}{(R + R_A)\ 2\pi\ C}$$

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Figure 17. Butterworth Filter – 2nd Order

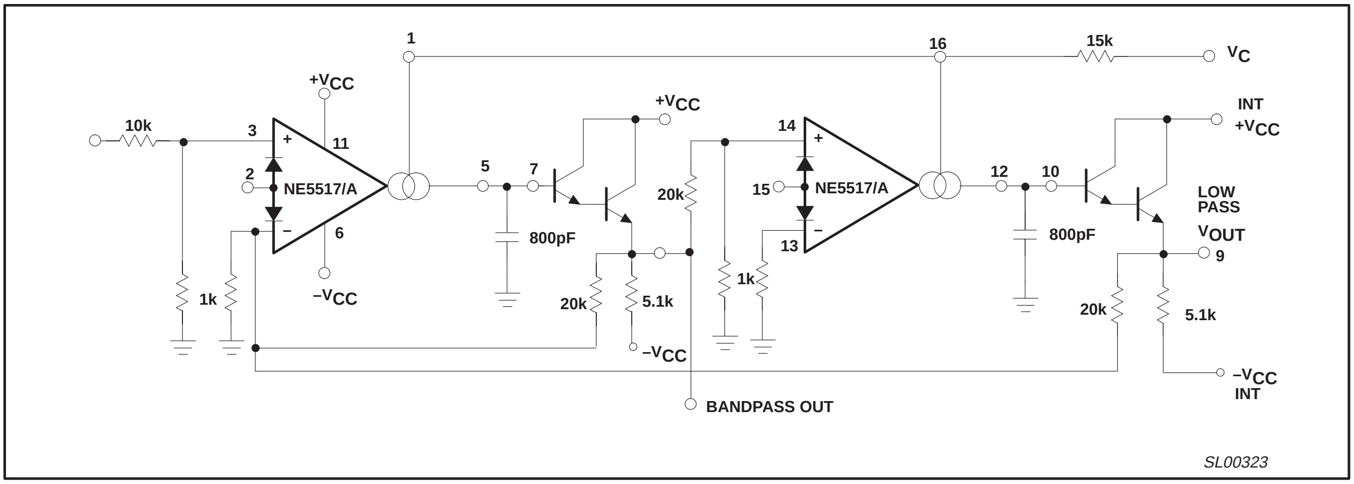


Figure 18. State Variable Filter

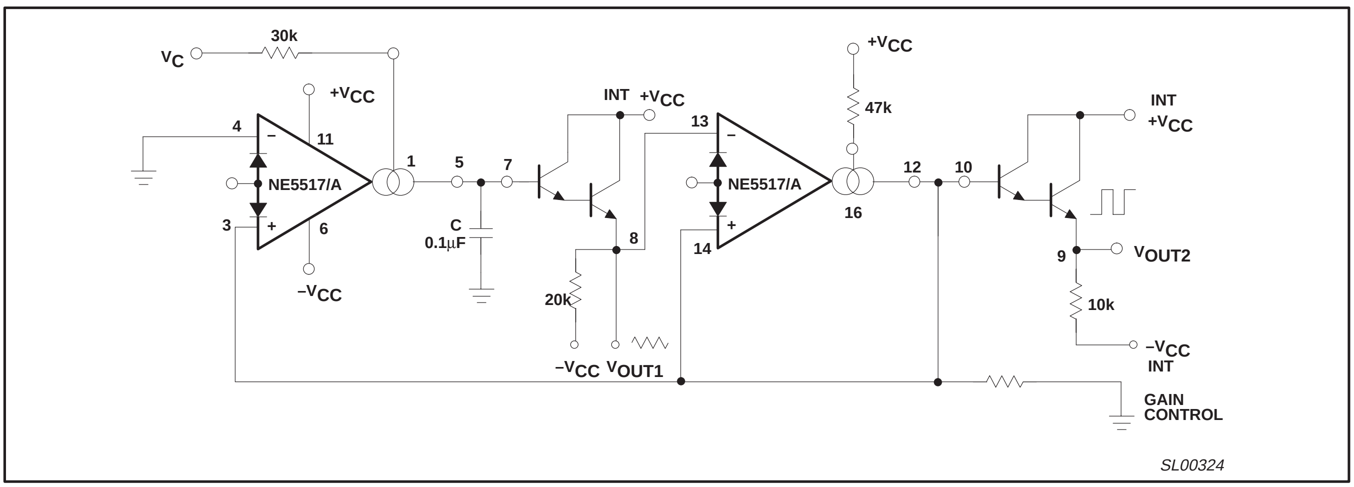
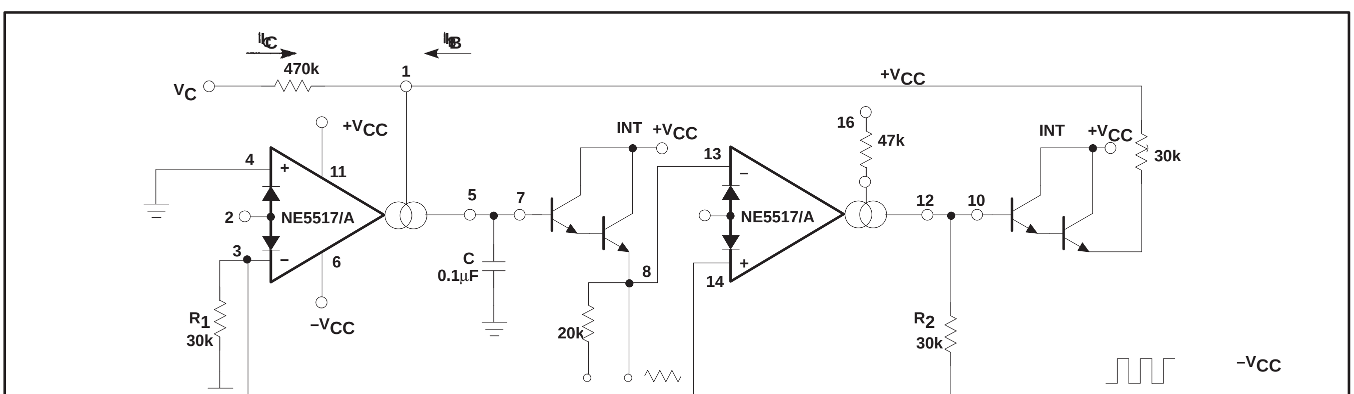


Figure 19. Triangle-Square Wave Generator (VCO)

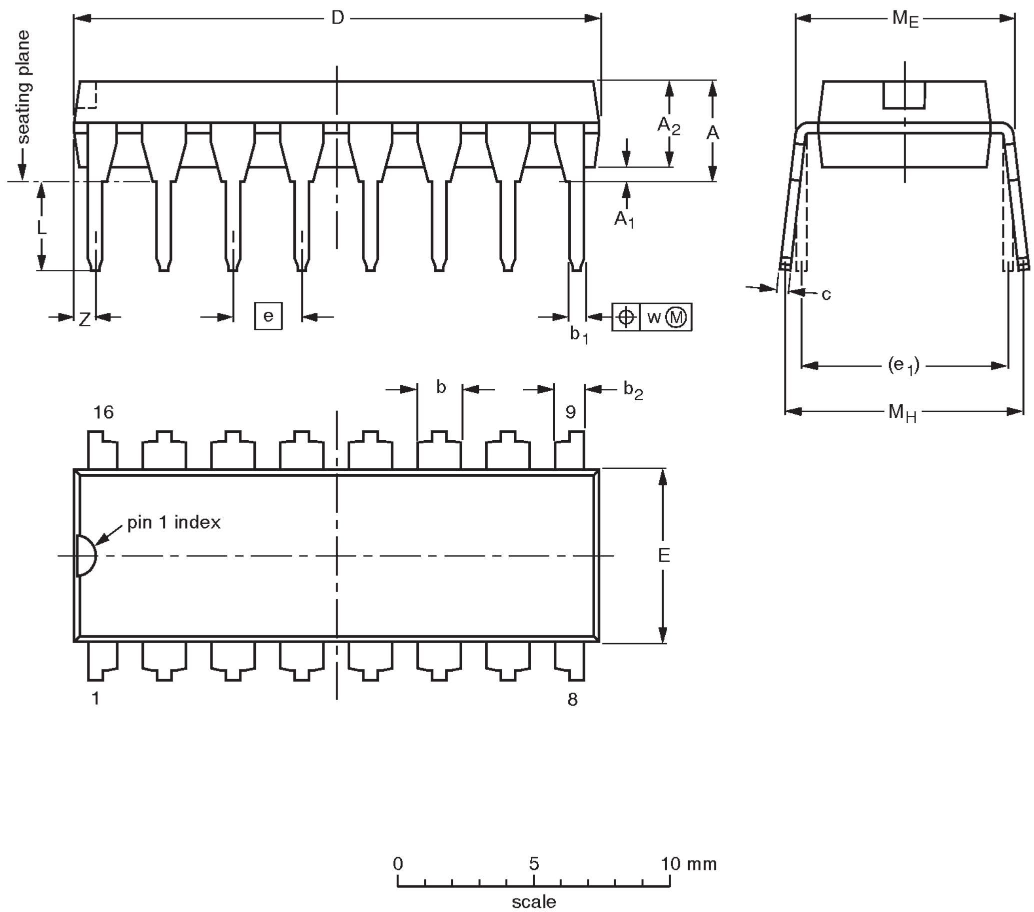


NOTE:

$$V_{PK} = \frac{(V_C - 0.8)\ R_1}{R_1 + R_2} \quad T_H = \frac{2V_{PK} \times C}{I_B} \quad T_L = \frac{2V_{PK} \times C}{I_C} \quad f_{OSC} \frac{I_C}{2V_{PK} \times C} \quad I_C < < I_B$$

Figure 20. Sawtooth Pulse VCO

DIP16: plastic dual in-line package; 16 leads (300 mil) **SOT38-4**

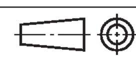


DIMENSIONS (inch dimensions are derived from the original mm dimensions)

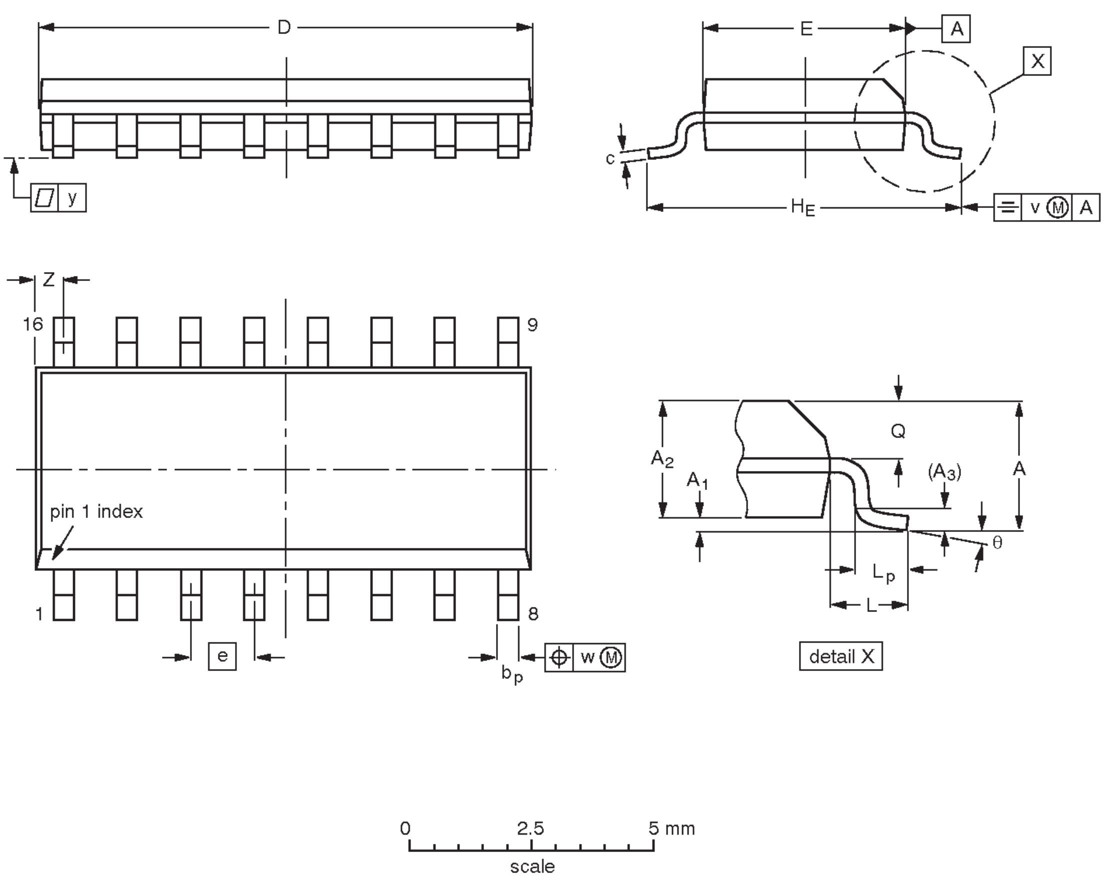
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						~~92-11-17~~ 95-01-14

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07	MS-012				~~97-05-22~~ 99-12-27

NOTES

Data sheet status

Data sheet status [1]	Product status [2]	Definitions
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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