CD4046B Phase-Locked Loop: A Versatile Building Block for Micropower Digital and Analog Applications

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ABSTRACT

Applications of the CD4046B phase-locked loop device, such as FM demodulation, FSK demodulation, tone decoding, frequency multiplication, signal conditioning, clock synchronization, and frequency synthesis, are discussed. The monolithic-form low-power-consumption CD4046B particularly is desirable for use in portable battery-powered equipment.

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1 Introduction

Phase-locked loops (PLLs), especially in monolithic form, have significantly increased use in signal-processing and digital systems. Frequency modulation (FM) demodulation, frequency shift keying (FSK) demodulation, tone decoding, frequency multiplication, signal conditioning, clock synchronization, and frequency synthesis are some of the many applications of a PLL. The PLL described in this application report is the CD4046B, which consumes only 600 μW of power at 10 kHz, a reduction in power consumption of 160 times when compared to the 100 mW required by similar monolithic bipolar PLLs. This power reduction has particular significance for portable battery-operated equipment. This application report discusses the basic fundamentals of PLLs, and presents a detailed technical description of the CD4046B, as well as some of its applications.

2 Review of PLL Fundamentals

The basic PLL system is shown in Figure 1. The system consists of three parts: phase comparator, low-pass filter (LPF), and voltage-controlled oscillator (VCO). All parts are connected to form a closed-loop frequency-feedback system.

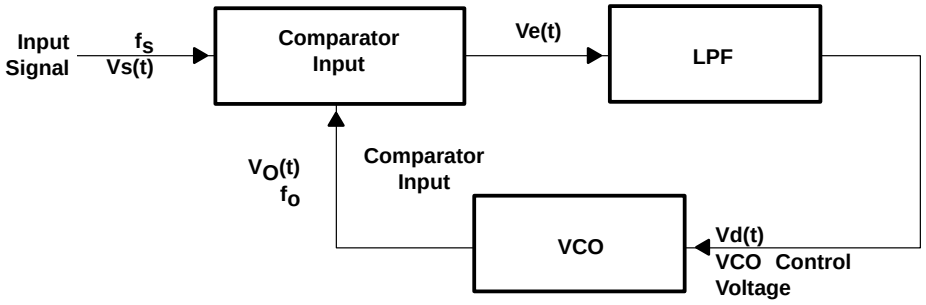


Figure 1. PLL Block Diagram

With no signal input applied to the PLL system, the error voltage at the output of the phase comparator is zero. The voltage, Vd(t), from the LPF also is zero, which causes the VCO to operate at a set frequency, f_O, called the center frequency. When an input signal is applied to the PLL, the phase comparator compares the phase and frequency of the signal input with the VCO frequency and generates an error voltage proportional to the phase and frequency difference of the input signal and the VCO. The error voltage, Ve(t), is filtered and applied to the control input of the VCO. Vd(t) varies in a direction that reduces the frequency difference between the VCO and signal-input frequency. When the input frequency is sufficiently close to the VCO frequency, the closed-loop nature of the PLL forces the VCO to lock in frequency with the signal input; i.e., when the PLL is in lock, the VCO frequency is identical to the signal input, except for a finite phase difference. The range of frequencies over which the PLL can maintain this locked condition is defined as the lock range of the system. The lock range always is larger than the band of frequencies over which the PLL can acquire a locked condition with the signal input. This latter band of frequencies is defined as the capture range of the PLL system.

3 CD4046B PLL Technical Description

Figure 2 shows a block diagram of the CD4046B, which has been implemented on a single monolithic integrated circuit. The PLL structure consists of a low-power, linear VCO and two different phase comparators, having a common signal-input amplifier and a common comparator input. A 5.2-V Zener diode is provided for supply regulation, if necessary. The VCO can be connected either directly or through frequency dividers to the comparator input of the phase comparators. The LPF is implemented through external parts because of the radical configuration changes from application to application and because some of the components cannot be integrated. The CD4046B is available in 16-lead ceramic dual-in-line packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead small outline package (NSR suffix) and in chip form (H suffix).

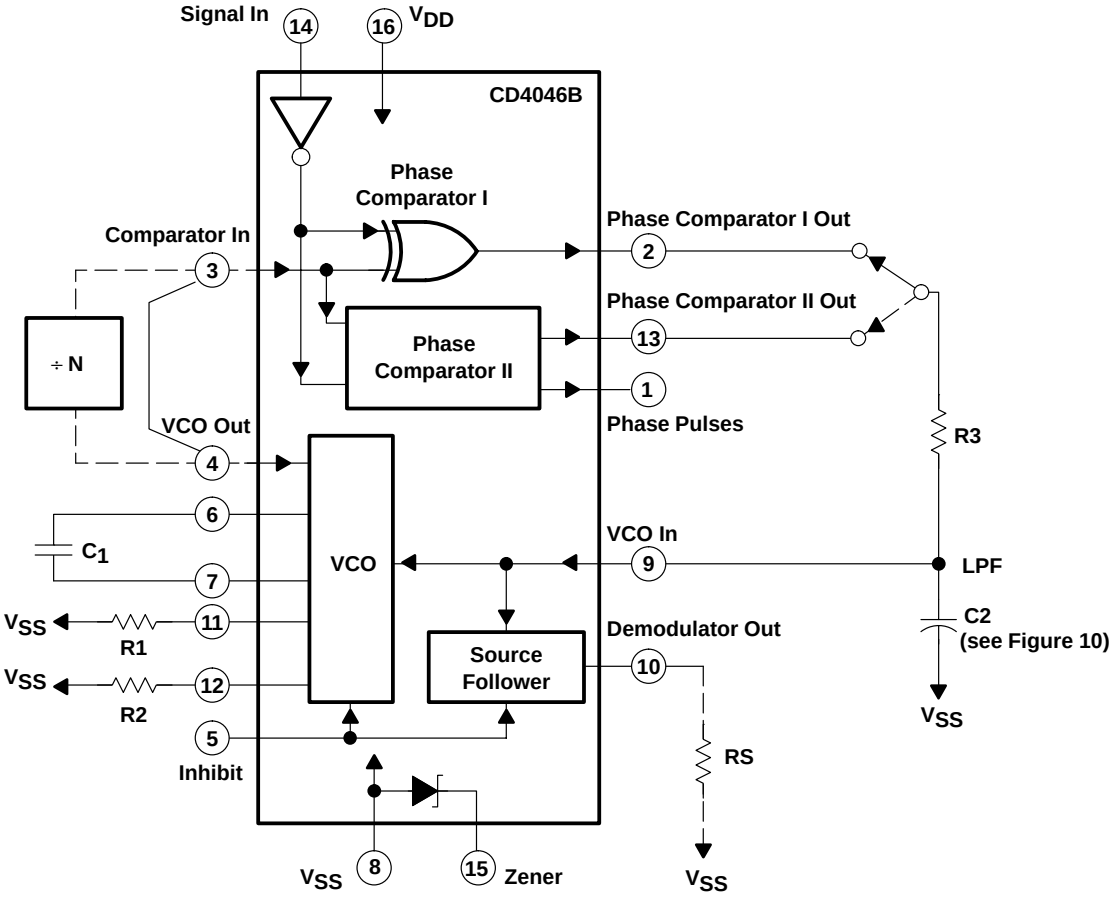


Figure 2. CD4046B Block Diagram

3.1 Phase Comparators

Most PLL systems utilize a balanced mixer, composed of well-controlled analog amplifiers for the phase-comparator section. The CD4046B design employs digital-type phase comparators (see Figure 3). Both phase comparators are driven by a common-input amplifier configuration composed of a bias stage and four inverting-amplifier stages. The phase-comparator signal input (terminal 14) can be direct coupled, provided the signal swing is within CMOS logic levels [logic 0 ≤ 30% (V_{DD}–V_{SS}), logic 1 ≥ 70% (V_{DD}–V_{SS})]. For smaller input signal swings, the signal must be capacitively coupled to the self-biasing amplifier at the signal input to ensure an overdriven digital signal into the phase comparators.

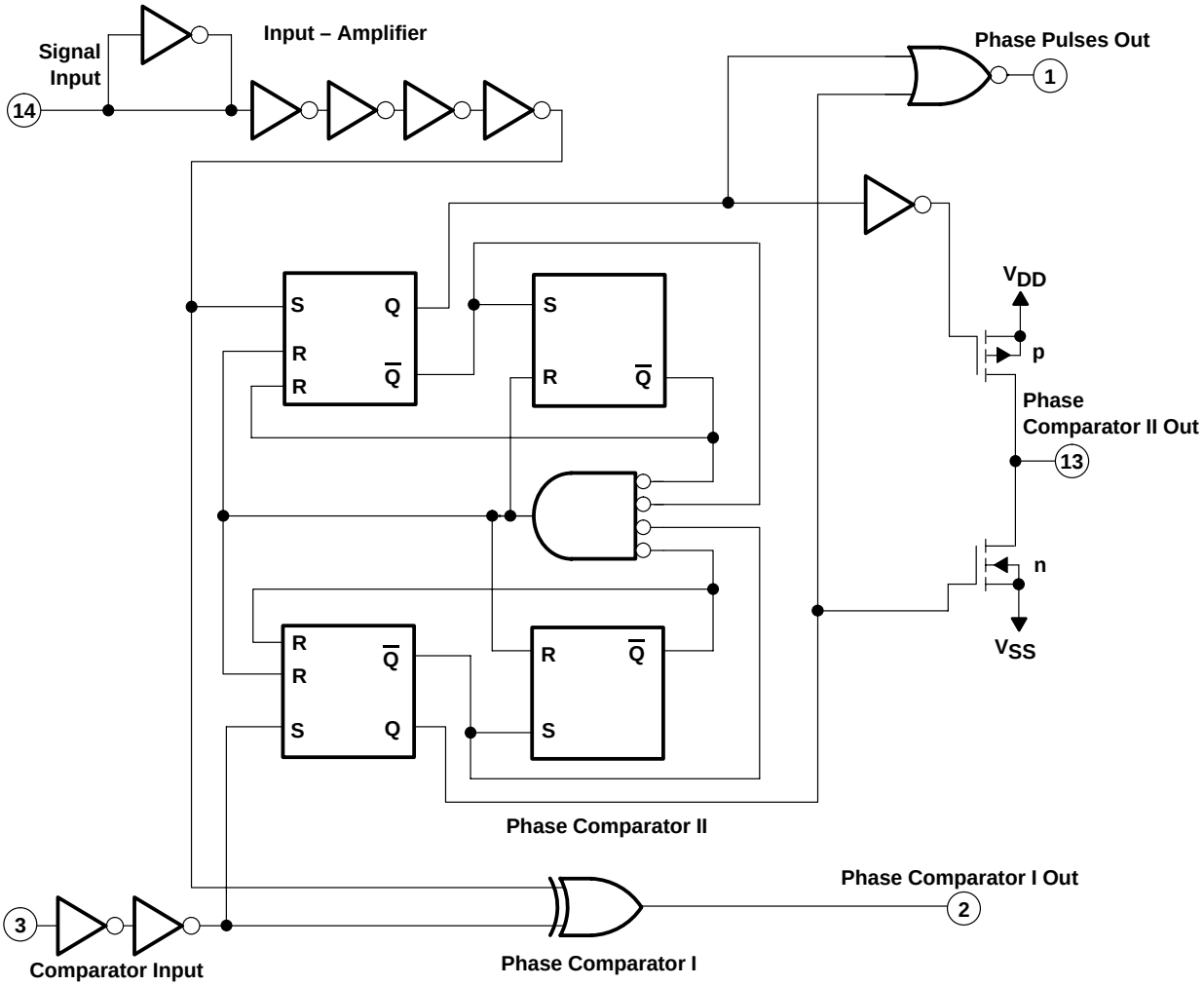


Figure 3. CD4046B Phase-Comparator Section Schematic

Phase comparator I is an exclusive-OR network that operates analogously to an overdriven balanced mixer. To maximize the lock range, the signal- and comparator-input frequencies must have 50% duty cycle. With no signal or noise on the signal input, this phase comparator has an average output voltage equal to $V_{DD}/2$. The LPF connected to the output of phase comparator I supplies the averaged voltage to the VCO input and causes the VCO to oscillate at the center frequency (f_0). With phase comparator I, the range of frequencies over which the PLL can acquire lock (capture range) is dependent on the LPF characteristics and can be made as large as the lock range.

Phase comparator I enables a PLL system to remain in lock despite high amounts of noise in the signal input.

One characteristic of this type of phase comparator is that it can lock onto input frequencies that are close to harmonics of the VCO center frequency. A second characteristic is that the phase angle between the signal and the comparator input varies between 0 degree and 180 degrees, and is 90 degrees at the center frequency. Figure 4 shows the typical, triangular, phase-to-output response characteristic of phase comparator I. Typical waveforms for a CD4046B employing phase comparator I in locked condition of f_0 is shown in Figure 5.

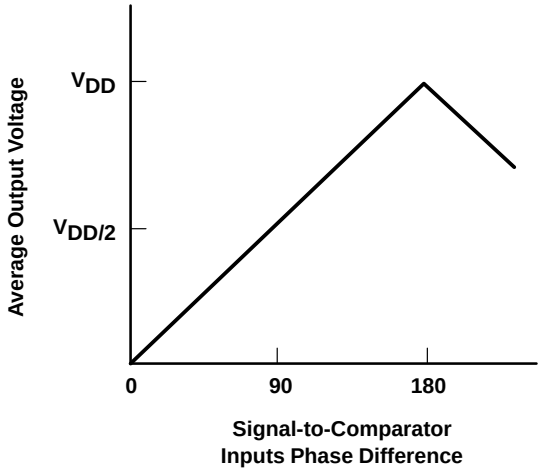


Figure 4. Phase Comparator I Characteristics at LPF Output

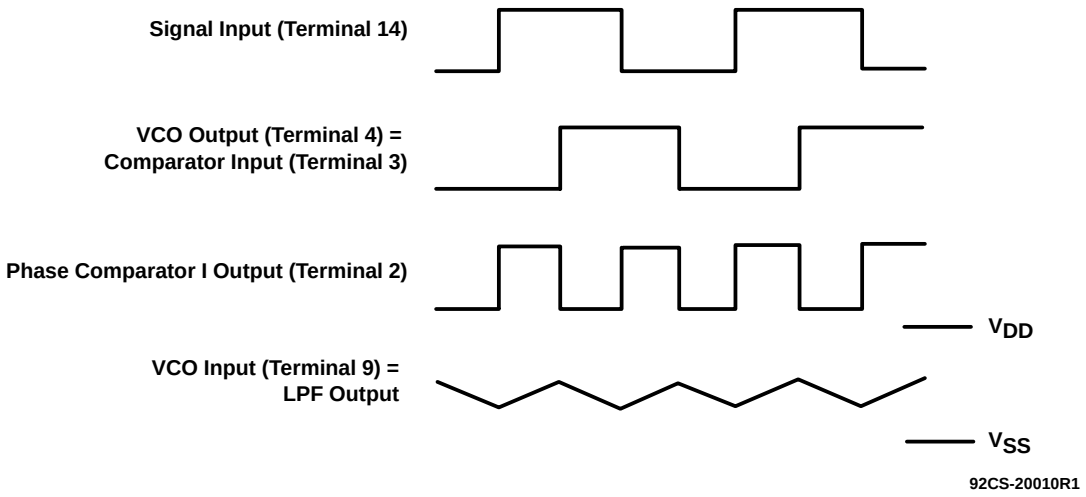
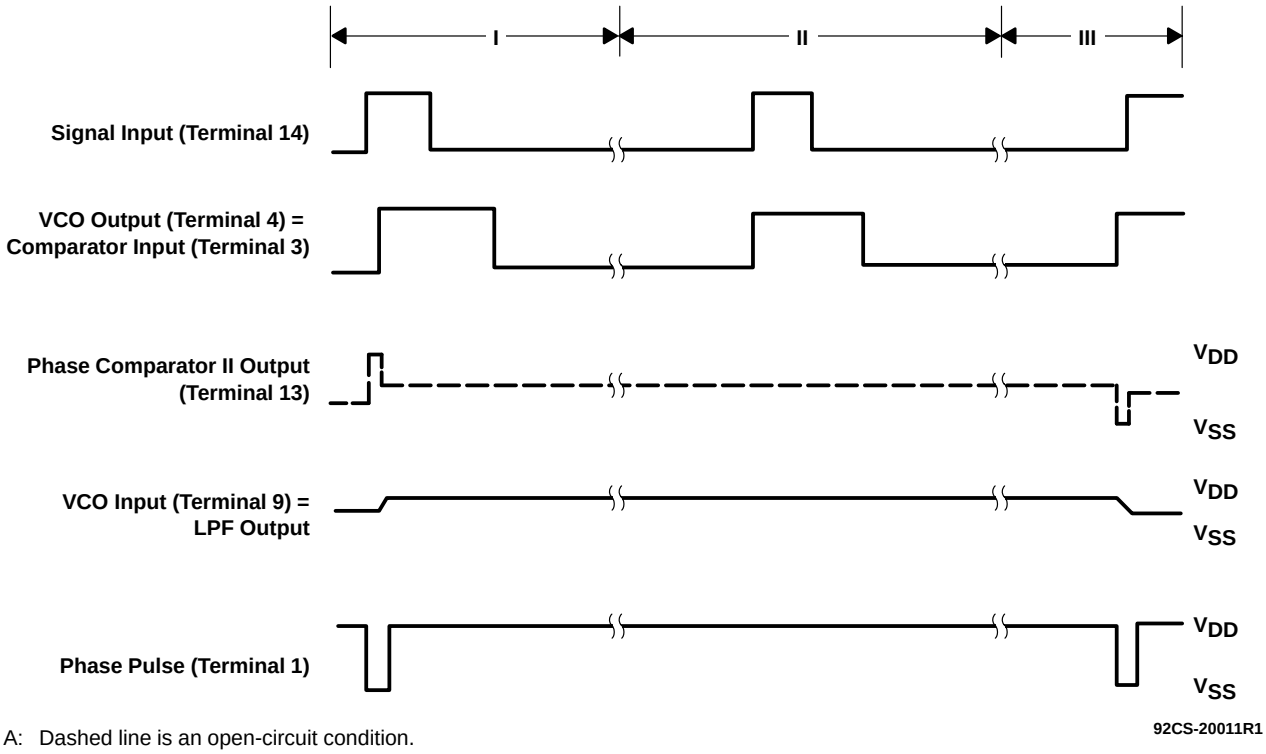


Figure 5. Typical Waveforms for the CD4046B Employing Phase Comparator I in Locked Condition of f_o

Phase comparator II is an edge-controlled digital memory network. It consists of four flip-flop stages, control gating, and a 3-state output circuit comprising p and n drivers having a common output node (see Figure 3). When the p-MOS or n-MOS drivers are on, they pull the output up to V_{DD} or down to V_{SS}, respectively. This type of phase comparator acts only on the positive edges of the signal- and comparator-input signals. The duty cycles of the signal and comparator inputs are not important because positive transitions control the PLL system that uses this type of comparator. If the signal-input frequency is higher than the comparator-input frequency, the p-MOS output driver is maintained on continuously. If the signal-input frequency is lower than the comparator-input frequency, the n-MOS output driver is maintained on continuously. If the signal- and comparator-input frequencies are the same, but the signal input lags the comparator input in phase, the n-MOS output driver is maintained on for a time corresponding to the phase difference. If the signal- and comparator-input frequencies are the same, but the signal input leads the comparator input in phase, the p-MOS output driver is maintained on for time corresponding to the phase difference. Subsequently, the capacitor voltage of the LPF connected to this type of phase comparator is adjusted until the signal and comparator input are equal in both phase and frequency. At this stable operating point, both p-MOS and n-MOS output drivers remain off, and the phase-comparator output becomes an open circuit and holds the voltage on the capacitor of the LPF constant. Moreover, the signal at the phase-pulses output is at a high level, and can be used for indicating a locked condition. Thus, for phase comparator II, no phase difference exists between signal and comparator input over the full VCO frequency range. Moreover, the power dissipation due to the LPF is reduced when this type of phase comparator is used because both the p-MOS and n-MOS output drivers are off for most of the signal-input cycle. Note that the PLL lock range for this type of phase comparator is equal to the capture range, independent of the LPF. With no signal present at the signal input, the VCO is adjusted to its lowest frequency for phase comparator II. Figure 6 shows typical waveforms for a CD4046B employing phase comparator II in a locked condition.



NOTE A: Dashed line is an open-circuit condition.

Figure 6. Typical Waveforms for the CD4046B Employing Phase Comparator II in Locked Condition

Figure 7 shows the state diagram for phase comparator II; each circle represents a state of the comparator. The number at the top inside each circle represents the state of the comparator, while the logic state of the signal and comparator inputs, represented by a 0 or a 1, are given by the left and right numbers, respectively, at the bottom of each circle. The transitions from one state to another result from either a logic change on the signal input (I) or the comparator input (C). A positive transition and a negative transition are shown by an arrow pointing up or down, respectively. The state diagram assumes that only one transition on either the signal input or the comparator input occurs at any instant. States 3, 5, 9, and 11 represent the condition at the output of phase comparator II when the p-MOS driver is on, while states 2, 4, 10, and 12 represent the condition when the n-MOS driver is on. States 1, 6, 7, and 8 represent the condition when the output of phase comparator II is in its high-impedance state, i.e., both p and n devices are off and the phase-pulses output (terminal 1) is high. The condition at the phase-pulses output for all other states is low.

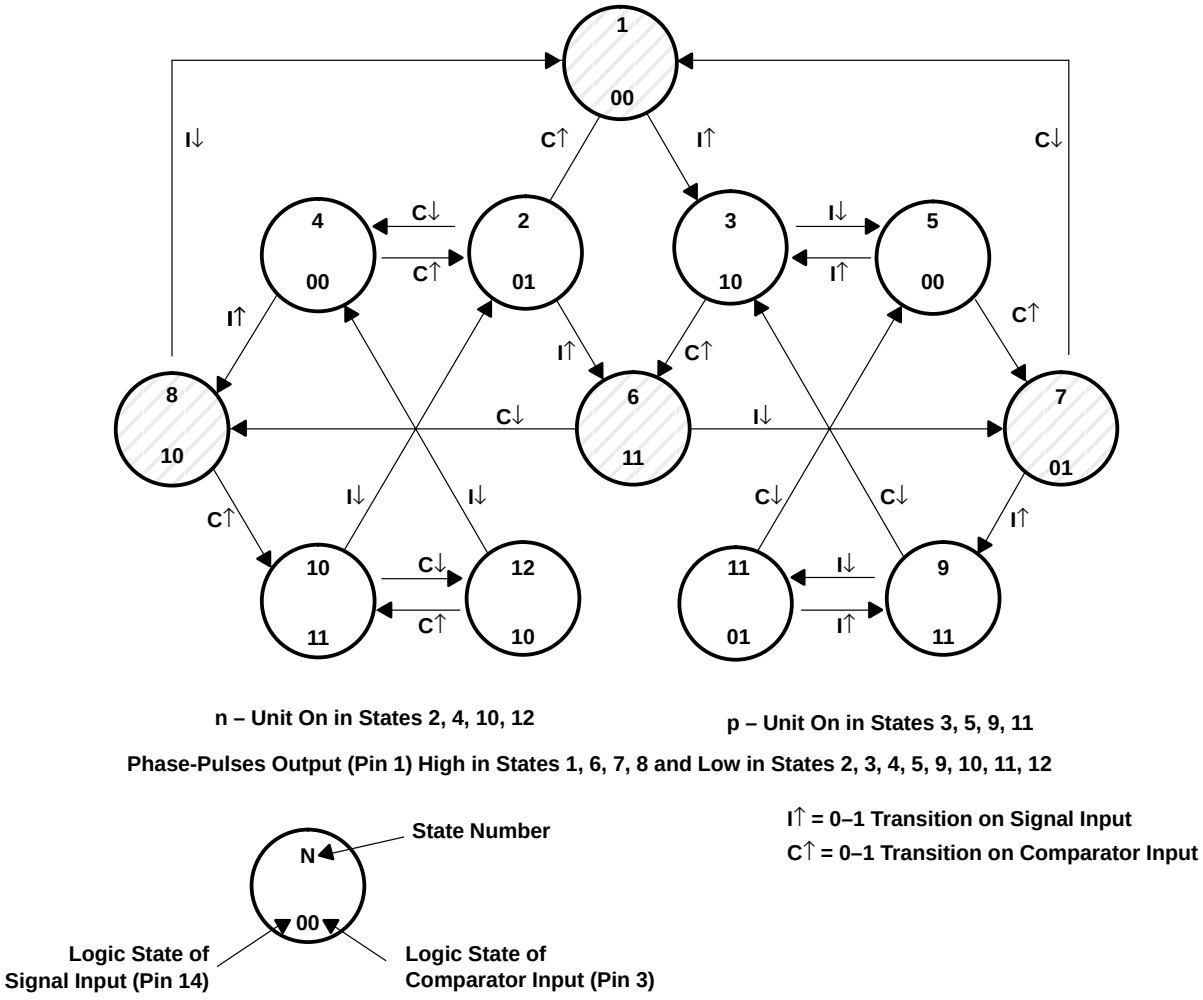


Figure 7. Phase Comparator II State Diagram

As an example of how to use the state diagram shown in Figure 7, consider the operation of phase comparator II in the locked condition shown in Figure 6. The waveforms shown in Figure 6 are broken up into three sections. Section I corresponds to the condition in which the signal input leads the comparator input in phase. Section II corresponds to a finite phase difference. Section III depicts the condition when the comparator input leads the signal input in phase. These three sections all correspond to a locked condition for the PLL, i.e., both signal- and comparator-input signals are of the same frequency, but differ slightly in phase.

Assume that both the signal inputs begin in the 0 state, and that phase comparator II initially is in its high-impedance output condition (state 1), as shown in Figures 7 and 6, respectively. The signal input makes a positive transition first, which brings phase comparator II to state 3. State 3 corresponds to the condition of the comparator in which the signal input is a 1, the comparator input is a 0, and the output p-device is on. The comparator input goes high next, while the signal input is high, thus, bringing the comparator to state 6, a high-impedance output condition. The signal input goes to zero next, while the comparator input is high, which corresponds to state 7. The comparator input goes low next, bringing phase comparator II back to state 1. As shown for section I, the p-device stays on for a time corresponding to the phase difference between the signal input and the comparator input. Starting in state 1 at the beginning of section III, the comparator input goes high first, while the signal input is low, bringing the comparator to state 2. Following the example given for section 1, the comparator proceeds from state 2 to states 6 and 8, then back to state 1. The output of phase comparator II for section III corresponds to the n-device being on for a time corresponding to the phase difference between the signal and comparator inputs.

The state diagram of phase comparator II describes all modes of operation of the comparator for any input condition in a PLL.

3.2 Voltage-Controlled Oscillator (VCO)

Figure 8 shows the schematic diagram of the VCO. To ensure low system-power dissipation, it is desirable that the LPF consume little power. For example in an RC filter, this requirement dictates that a high-value R and a low-value C be used. However, the VCO input must not load down or modify the characteristics of the LPF. Because the VCO design shown in Figure 8 was an n-MOS input configuration having practically infinite input resistance, a great degree of freedom is allowed in selecting the LPF components.

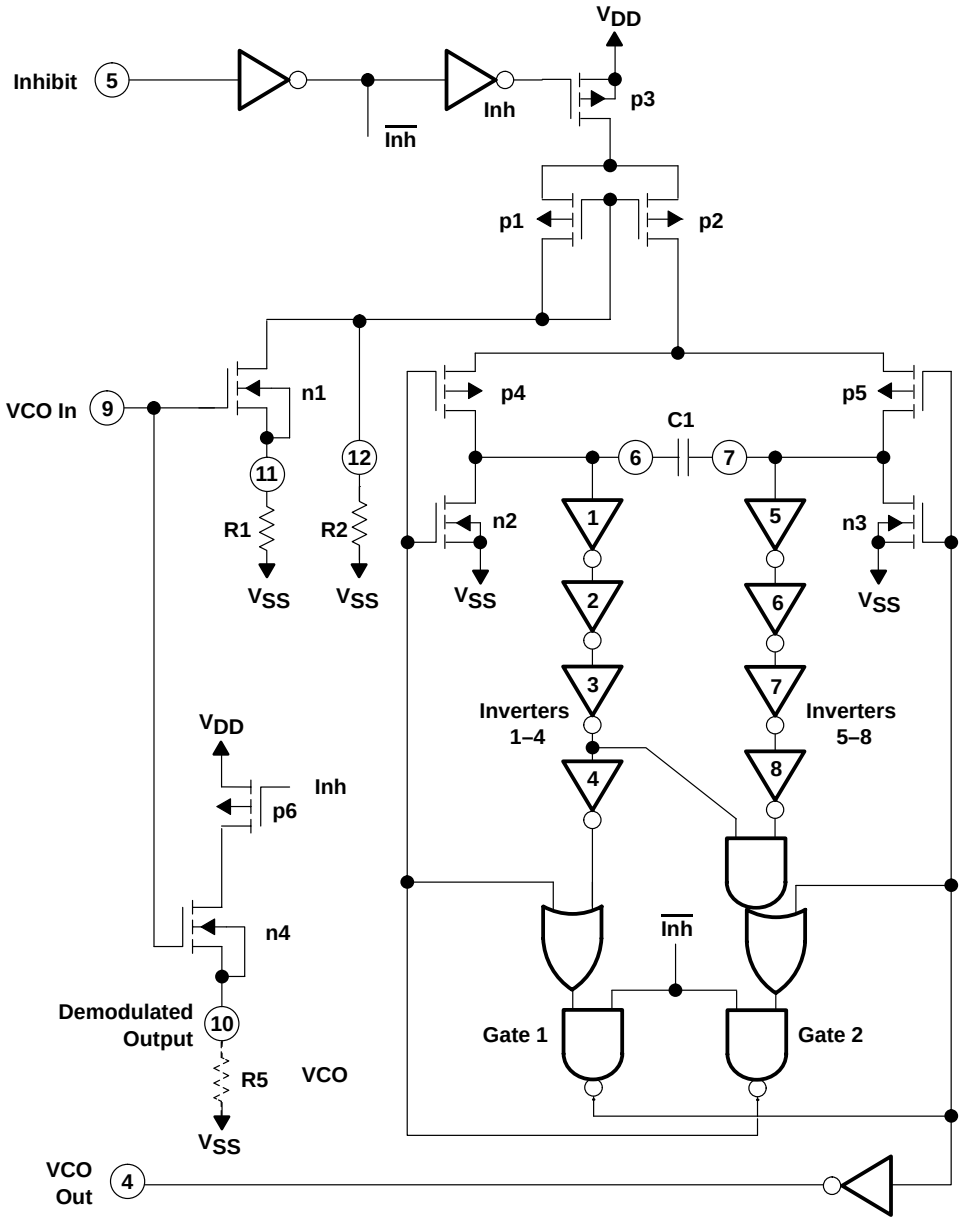


Figure 8. CD4046B VCO Section Schematic

The VCO circuit shown in Figure 8 operates as follows; when the inhibit input is low, p3 is turned full on, effectively connecting the sources of p1 and p2 to V_{DD}, and gates 1 and 2 are permitted to function as NOR-gate flip-flops. n1 and external resistor R1 form a source-follower configuration. As long as the resistance of R1 is at least an order of magnitude greater than the on resistance of n1 (greater than 10 kΩ), current through R1 is linearly dependent on the VCO input voltage. This current flows through p1, which, together with p2, forms a current-mirror network. External resistor R2 adds an additional constant current through p1; this current offsets the VCO operating frequency for VCO input signals of 0 volts. In the current-mirror network, the current of p2 is effectively equal to the current through p1, independent of the drain voltage at p2. (This condition is true, provided p2 is maintained in saturation. In the circuit in Figure 8, p2 is saturated under all possible operating conditions and modes.) The set/reset flip-flop composed of gates 1 and 2 turns on either p4 and n3 or p5 and n2. One side of external capacitor C1 is, therefore, held at ground, while the other side is charged by the constant current supplied by p2. As soon as C1 charges to the point at which the transfer point of inverters 1 or 5 is reached, the flip-flop changes state. The charged side of the capacitor now is pulled to ground. The other side of the capacitor goes negative and discharges rapidly through the drain diode of the off n device. Subsequently, a new half cycle starts. Because inverters 1 and 5 have the same transfer points, the VCO has a 50% duty cycle. Inverters 1–4 and 5–8 serve several purposes:

- Shape the slow-input ramp from capacitor C1 to a fast waveform at the flip-flop input stage
- Maintain low power dissipation through the use of high-impedance devices at inverters 1 and 5 (slow-input waveforms)
- Provide four inverter delays before removal of the set/reset flip-flop triggering pulse to ensure proper switching action

In order not to load the LPF, a source-follower output of the VCO input voltage is provided (demodulated output). If this output is used, a load resistor (RS) of 10 kΩ, or more, should be connected from this terminal to ground. If unused, this terminal should be left open. A logic 0 on the inhibit input enables the VCO and the source follower, while a logic 1 turns off the VCO and source follower to minimize standby power consumption.

3.3 CD4046B Performance Summary

The maximum ratings for the CD4046B, as well as its general operating and performance characteristics, are shown in Table 1. The VCO and comparator characteristics are shown in Tables 2 and 3, respectively. Table 4 summarizes some useful formulas as a guide for approximating the values of external components for the CD4046B in a PLL system. When using Table 4, note that frequencies are in kilohertz, resistance is in kilohms, and capacitance is in microfarads. The selected external components must be within the following ranges:

$10\ k\Omega = \leq R1, R2, RS \leq 1\ M\Omega$
$C1 \geq 100\ pF$ at $V_{DD} \geq 5\ V$
$C1 \geq 50\ pF$ at $V_{DD} \geq 10\ V$

Table 1. Maximum Ratings and General Operating Characteristics

Maximum Ratings, Absolute-Maximum Values

Storage temperature range . . . . . –65°C to 150°C
Operating temperature range: Ceramic package types . . . . . –55°C to 125°C
Plastic package types . . . . . –40°C to 85°C
DC supply voltage range ($V_{DD} – V_{SS}$) . . . . . –0.5 V to 15 V
Device dissipation (per package) . . . . . 200 mW
All inputs . . . . . $V_{SS} \leq V_I \leq V_{DD}$
Recommended dc supply voltage range ($V_{DD} – V_{SS}$) . . . . . 5 V to 15 V
Recommended input voltage swing . . . . . V_{DD} to V_{SS}

General Characteristics (Typical Values at $V_{DD} – V_{SS}$ = 10 V and T_A = 25°C)

Operating supply voltage range ($V_{DD} – V_{SS}$) . . . . . 5 V to 15 V
Operating supply current: Inhibit = 0: f_0 = 10 kHz, V_{DD} = 5 V . . . . . 70 μW
C1 = 0.0001 μF: R1 = 1 MΩ, f_0 = 10 kHz, V_{DD} = 10 V . . . . . 600 μW
Inhibit = 1 . . . . . 25 μA

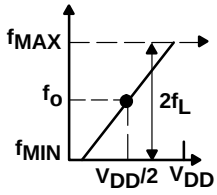
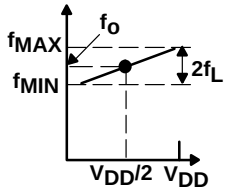
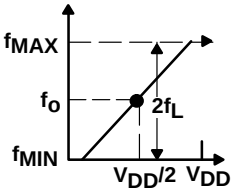
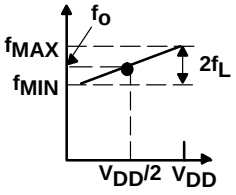
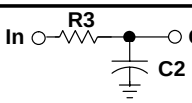
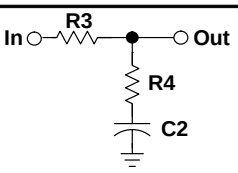
Table 2. VCO Electrical Characteristics

VCO CHARACTERISTICS		TYPICAL VALUES AT $V_{DD} – V_{SS}$ = 10 V AND T_A = 25°C
Maximum frequency		1.2 MHz
Temperature stability		600 ppm/°C
Linearity (V_{VCO} in = 5 V ± 2.5 V)		1%
Center frequency		Programmable with R1 and C1
Frequency range		Programmable with R1, R2, and C2
Input resistance		10^{12}
Output voltage		10 Vp-p
Duty cycle		50%
Rise and fall times		50 ns
Output current capability	Logic 1: Drive at V_O 9.5 V	–1.8 mA
	Logic 0: Sink at V_O 0.5 V	2.6 mA
Demodulated output: Offset voltage ($V_{VCO\ in} – V_{DEMOD\ out}$) at 1 mA		1.5 V

Table 3. Comparator Electrical Characteristics

COMPARATOR CHARACTERISTICS	TYPICAL VALUES AT $V_{DD} - V_{SS}$ = 10 V AND T_A = 25°C
Signal Input	
Input impedance	400 kΩ
Input sensitivity	
AC coupled	400 mV
DC coupled	Logic 0: ≤30% ($V_{DD} - V_{SS}$)
	Logic 1: ≥70% ($V_{DD} - V_{SS}$)
Comparator-input levels (terminal 3)	Logic 0: ≤30% ($V_{DD} - V_{SS}$)
	Logic 1: ≥70% ($V_{DD} - V_{SS}$)
Output Current Capability	
Comparator I (terminal 2) and comparator II (terminal 13)	
Logic 1: Drive at V_O = 9.5 V	–1.8 mA
Logic 0: Sink at V_O = 0.5 V	2.6 mA
Comparator II phase pulses (terminal 1)	
Logic 1: Drive at V_O = 9.5 V	–1.8 mA
Logic 0: Sink at V_O = 0.5 V	1.4 mA

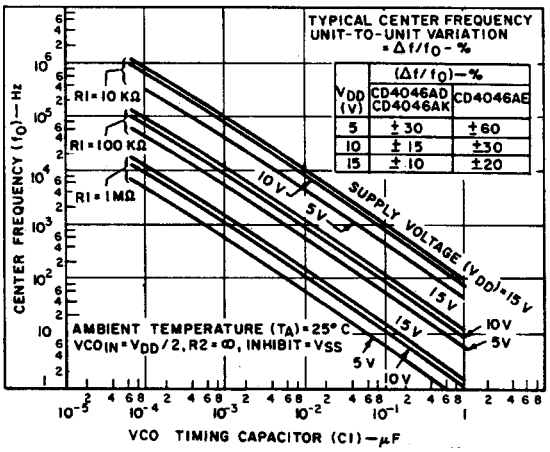
Table 4. Phase Comparator Comparison

CHARACTERISTICS	USING PHASE COMPARATOR I		USING PHASE COMPARATOR II	
	VCO WITHOUT OFFSET R2 = ∞	VCO WITH OFFSET	VCO WITHOUT OFFSET R2 = ∞	VCO WITH OFFSET
VCO frequency	 VCO Input Voltage	 VCO Input Voltage	 VCO Input Voltage	 VCO Input Voltage
For no signal input	VCO in PLL system adjusts to center frequency, f_o		VCO in PLL system adjusts to lowest operating frequency, f_{min}	
Frequency-lock range, $2f_L$	$2f_L$ = full VCO frequency range $2f_L = f_{max} - f_{min}$			
Frequency capture range, $2f_C$	 See Notes 1 and 2 $2f_C \approx \frac{1}{\tau 1}\sqrt{\frac{2\pi f_L}{\tau 1}}$ $\tau 1 = R3 \times C2$		$f_C = f_L$	
Loop filter-component selection	 For $2f_C$, see Note 2			
Phase angle between signal and comparator inputs	90 degrees at center frequency (f_o), approximating 0 degree and 180 degrees at ends of lock range ($2f_L$)		Always 0 degrees in lock	
Locks on harmonics of center frequency	Yes		No	
Signal input noise rejection	High		Low	
VCO component selection	– Given: f_o – Use f_o with Figure 9a to determine R1 and C1	– Given: f_o and f_L – Calculate f_{min} from the equation $f_{min} = f_o - f_L$ – Use f_{min} with Figure 9b to determine R2 and C1 – Calculate $\frac{f_{max}}{f_{min}}$ from the equation $\frac{f_{max}}{f_{min}} = \frac{f_o + f_L}{f_O - f_L}$ – Use $\frac{f_{max}}{f_{min}}$ with Figure 9C to determine ratio R2/R1 to obtain R1	– Given: f_{max} – Calculate f_o from the equation $f_o = \frac{f_{max}}{2}$ – Use f_o with Figure 9a to determine R1 and C1	– Given: f_{min} and f_{max} – Use f_{min} with Figure 9b to determine R2 and C1 – Calculate $\frac{f_{max}}{f_{min}}$ – Use $\frac{f_{max}}{f_{min}}$ with Figure 9c to determine the ratio R2/R1 to obtain R1

NOTES: 1. F. Gardner, *Phase-Lock Techniques*, John Wiley and Sons, New York, 1966.
2. G.S. Moschytz, Miniaturized RC Filters Using PLL, *BSTJ,* May 1965.

In addition to the design information in Tables 1, 2, and 3, refer to Figure 9 for R1, R2, and C1 component selections. The use of Table 4 in designing a PLL system using the CD4046B for some familiar applications is discussed in the following paragraphs.

(a) Typical Center Frequency vs C1 for R1 = 10 kΩ, 100 kΩ, and 1 MΩ



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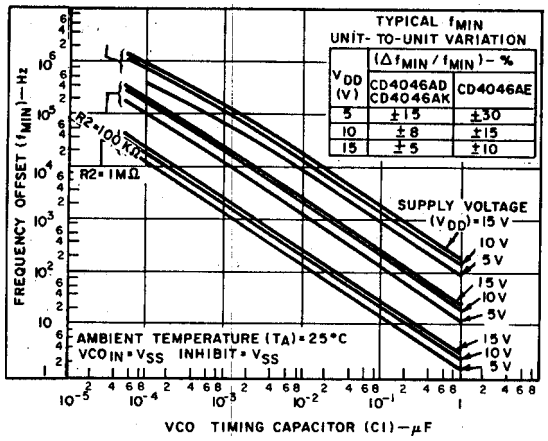
(b) Typical Frequency Offset vs C1 for R2 = 10 kΩ, 100 kΩ, and 1 MΩ



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(c) Typical f_{max}/f_{min} vs R2/R1

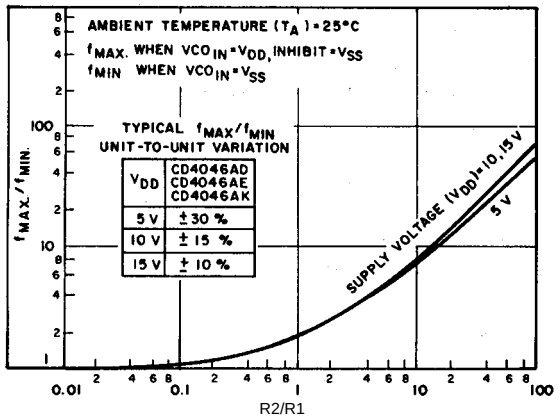

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Figure 9. Component-Selection Criteria

4 CD4046B PLL Applications

The CD4046B PLL is a versatile building block, suitable for a wide variety of applications, such as FM demodulators, frequency synthesizers, split-phase data synchronization and decoding, and PLL lock detection.

4.1 FM Demodulation

When a PLL is locked on an FM signal, the VCO tracks the instantaneous frequency of that signal. The VCO input voltage, which is the filtered error voltage from the phase detector, corresponds to the demodulated output. Figure 10 shows the connections of the CD4046B as an FM demodulator. For this example, an FM signal consisting of a 10-kHz carrier frequency was modulated by a 400-Hz audio signal. The total FM signal amplitude is 500 mV, therefore, the signal must be ac coupled to the signal input (terminal 14). Phase comparator I is used for this application because a PLL system with a center frequency equal to the FM carrier frequency is needed. Phase comparator I lends itself to this application also because of its high signal-input-noise-rejection characteristics.

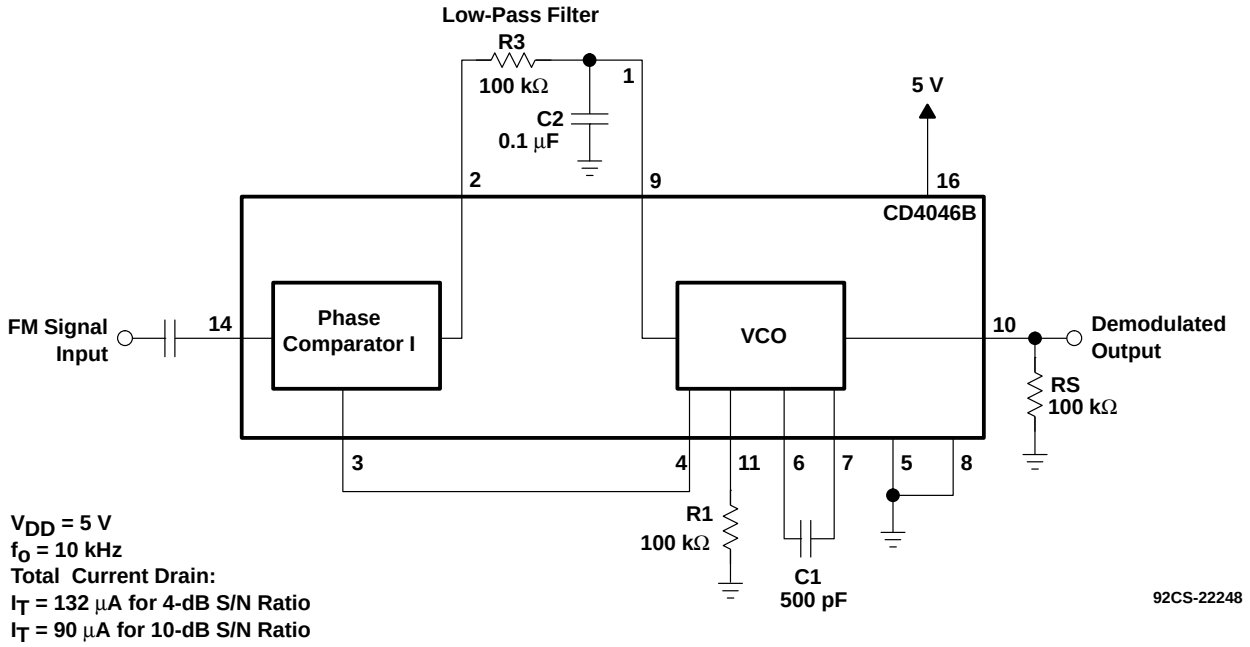

Figure 10. FM Demodulator

The formulas in Table 4 for phase comparator I with R2 = ∞ are used in the following considerations. The center frequency of the VCO is designed to be equal to the carrier frequency, 10 kHz. The 500-pF value of capacitor C1 was found by assuming R1 = 100 kΩ for a supply voltage of V_{DD} = 5 V.

These values determined the center frequency (f_0 = 10 kHz).

The PLL was set for a capture range of

$$f_c \approx \pm\left(\frac{1}{2\pi}\right)\left(\frac{2\pi f1}{R_3 C_2}\right) = \pm 0.4 \text{ kHz}$$

to allow for the deviation of the carrier frequency due to the audio signal. The components shown in Figure 10 for the LPF (R3 = 100 kΩ, C2 = 0.1 μF) determine this capture frequency.

The total current drain at a supply voltage of 5 V for this FM-demodulator application is 132 μA for a 4-dB S/N ratio on the signal input, and 90 μA for a 10-dB S/N ratio. Power consumption decreases because the signal-input amplifier goes into saturation at higher input levels.

Figure 11 shows the performance of the FM-demodulator circuit of Figure 10 at a 4-dB S/N ratio. The demodulated output is taken off the VCO-input source follower using resistor RS = 100 kΩ. The demodulation gain for this circuit is 250 mV/kHz.

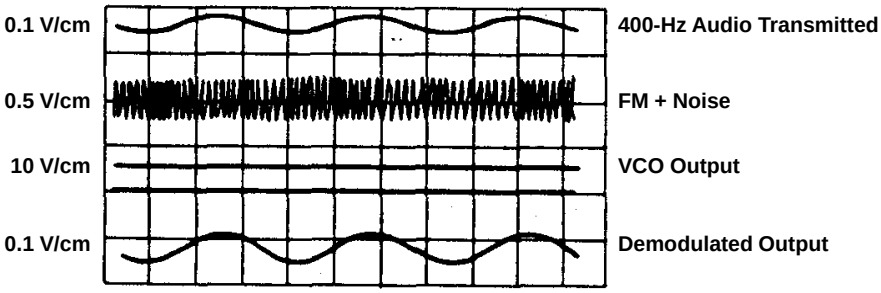

Figure 11. FM Demodulator Voltage Waveforms

4.2 Frequency Synthesizer

The PLL system can function as a frequency-selective frequency multiplier by inserting a frequency divider into the feedback loop between the VCO output and the comparator input. Figure 12 shows a low-frequency synthesizer with a programmable divider consisting of three decades. The frequency-divider modulus, N, can vary from 3 to 999, in steps of 1. When the PLL system is in lock, the signal and comparator inputs are at the same frequency, and f = N × 1 kHz.

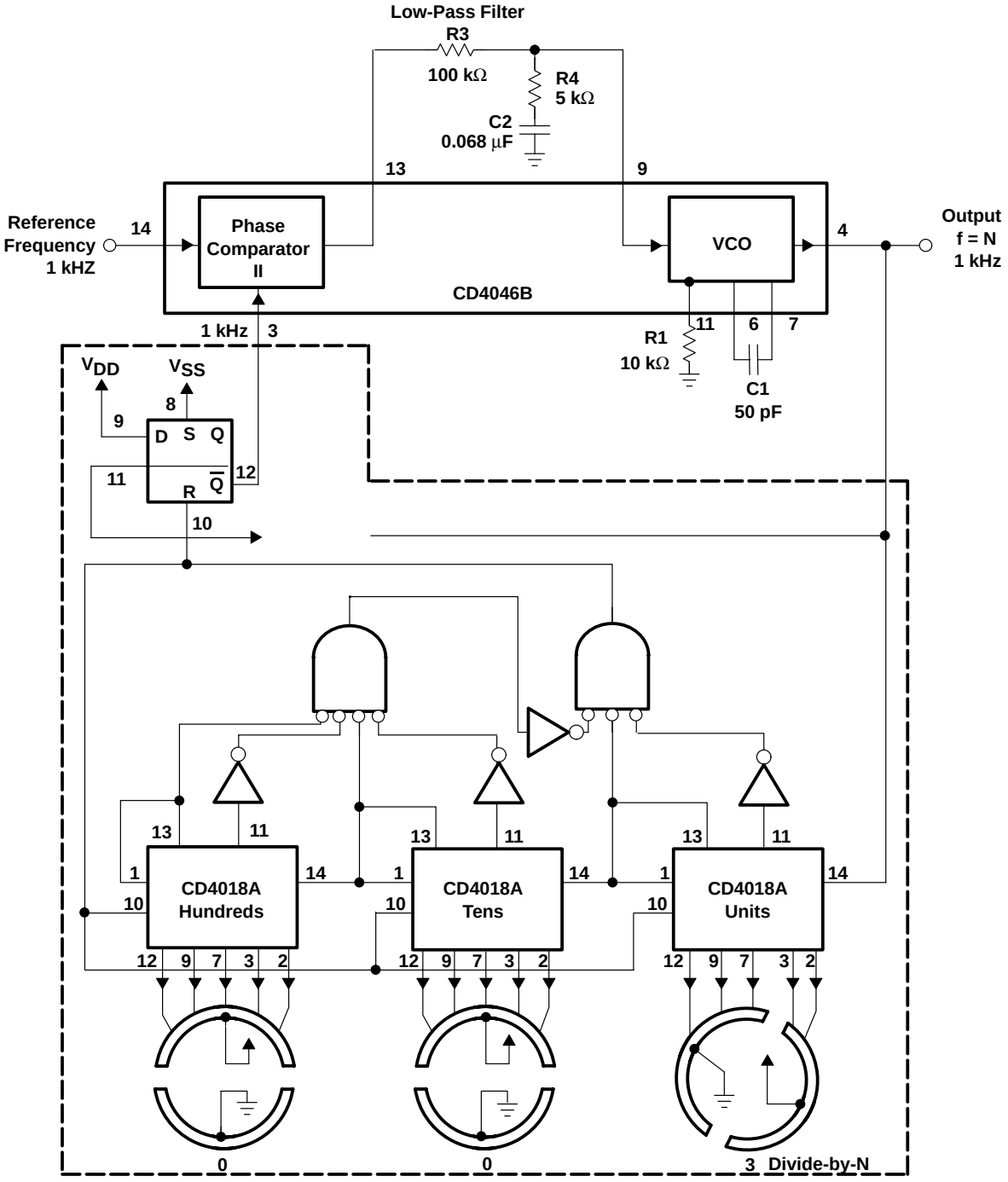

Figure 12. Low-Frequency Synthesizer With Three-Decade Programmable Divider

Therefore, the frequency range of this synthesizer is 3 kHz to 999 kHz in 1-kHz increments, which is programmable by the switch position of the divide-by-n counter.

Phase comparator II is used for this application because it will not lock on harmonics of the signal-input reference frequency (phase comparator I does lock on harmonics). Because the duty cycle of the output of the divide-by-n frequency divider is not 50%, phase comparator II lends itself directly to this application.

Using the formulas for phase comparator II shown in Table 4, the VCO is set up to cover a range of 0 MHz to 1.1 MHz. The LPF for this application is a two-pole, tag-lead filter that enables faster locking for step changes in frequency. Figure 13 shows the waveforms during switching between output frequencies of 3 kHz and 903 kHz. Figure 13 shows that the transient going toward 3 kHz on the VCO control voltage is overdamped, while the transient to 903 kHz is underdamped. This condition could be improved by changing the value of R3 in the LPF by adjusting the switch-position hundreds in the divide by-n counter.

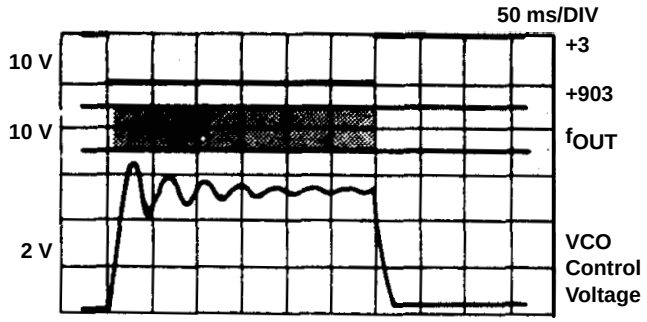

Figure 13. Frequency-Synthesizer Waveforms

4.3 Split-Phase Data Synchronization and Decoding

Figure 14 shows another application of the CD4046B for split-phase data synchronization and decoding. A split-phase data signal consists of a series of binary digits that occur at a periodic rate, as shown in waveform A in Figure 14. The weight of each bit, 0 or 1, is random, but the duration of each bit and, therefore, the periodic bit rate, essentially is constant. To detect and process the incoming signal, it is necessary to have a clock that is synchronous with the data bit rate. This clock signal must be derived from the incoming data signal. Phase-lock techniques can be utilized to recover the clock and the data. Timing information is contained in the data transitions, which can be positive or negative in direction, but both polarities have the same meaning for timing recovery. The phase of the signal determines the binary bit weight. A binary 0 or 1 is a positive or negative transition, respectively, during a bit interval in split-phase data signals.

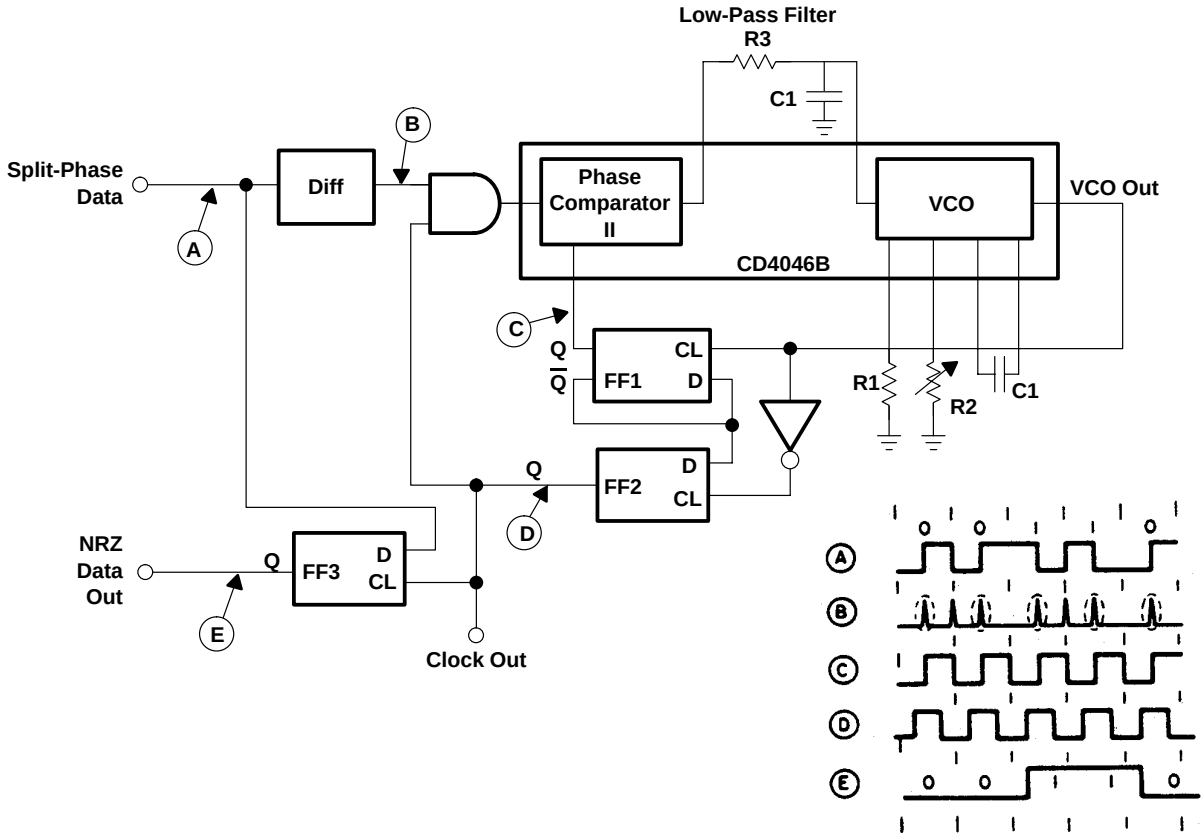

Figure 14. Split-Phase Data Synchronization and Decoding

As shown in Figure 14, the split-phase data input, A, is first differentiated to mark the locations of the data transitions. The differentiated signal, B, which is twice the bit rate, is gated into the CD4046B. Phase comparator II in the PLL is used because of its insensitivity to duty cycle on both the signal and comparator inputs. The VCO output is fed into the clock input of FF1, which divides the VCO frequency by two. During the on intervals, the PLL tracks the differentiated signal B. During the off intervals, the PLL remembers the last frequency present and still provides a clock output. The VCO output is inverted and fed into the clock input of FF2, whose data input is the inverted output of FF1. FF2 provides the necessary phase shift in signal C to obtain signal D, the recovered clock signal from the split-phase data transmission. The output of FF3, E, is the recovered binary information from the phase information contained in the split-phase data. Initial synchronization of this PLL system is accomplished by a string of alternating 0s and 1s that precede the data transmission.

4.4 PLL Lock Detection

In some applications that utilize a PLL, sometimes it is necessary to have an output indication of when the PLL is in lock. One of the simplest forms of lock-condition indication is a binary signal. For example, a 1 or a 0 output from a lock-detection circuit would correspond to a locked or unlocked condition, respectively. This signal could, in turn, activate circuitry using a locked PLL signal. This detection also could be used in FSK data transmissions in which digital information is transmitted by switching the input frequency between either of two discrete input frequencies, one corresponding to a digital 1 and the other to a digital 0.

Figure 15 shows a lock-detection scheme for the CD4046B. The signal input is switched between two discrete frequencies of 20 kHz and 10 kHz. The PLL system uses phase comparator II; the VCO bandwidth is set up for an f_{min} of 9.5 kHz and an f_{max} of 10.5 kHz. Therefore, the PLL locks and unlocks on the 10-kHz and 20-kHz signals, respectively. When the PLL is in lock, the output of phase comparator I is low, except for some very short pulses that result from the inherent phase difference between the signal and comparator inputs; the phase-pulses output (terminal 1) is high, except for some very small pulses resulting from the same phase difference. This low condition of phase comparator I is detected by the lock-detection circuit shown in Figure 15. Figure 16 shows the performance of this circuit when the input signal is switched between 20 kHz and 10 kHz. After about five input cycles, the lock detection signal goes high.

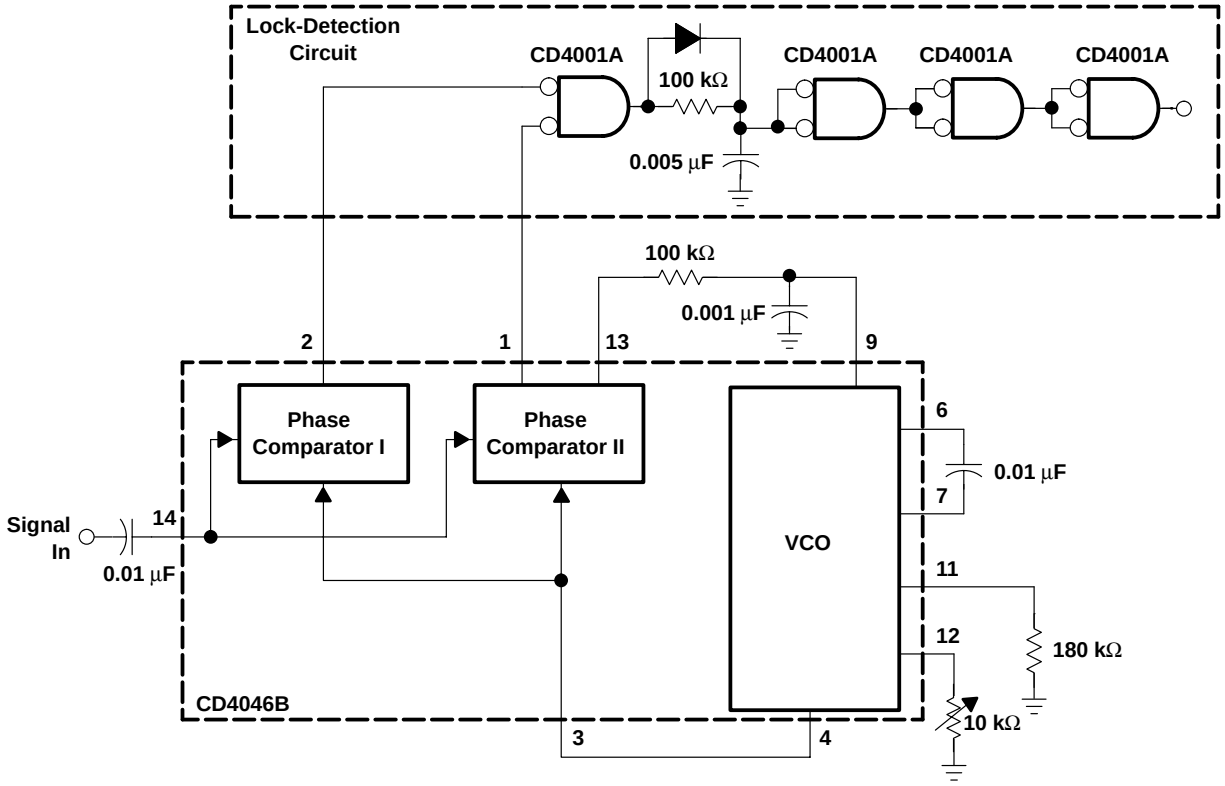

Figure 15. Lock-Detection Circuit

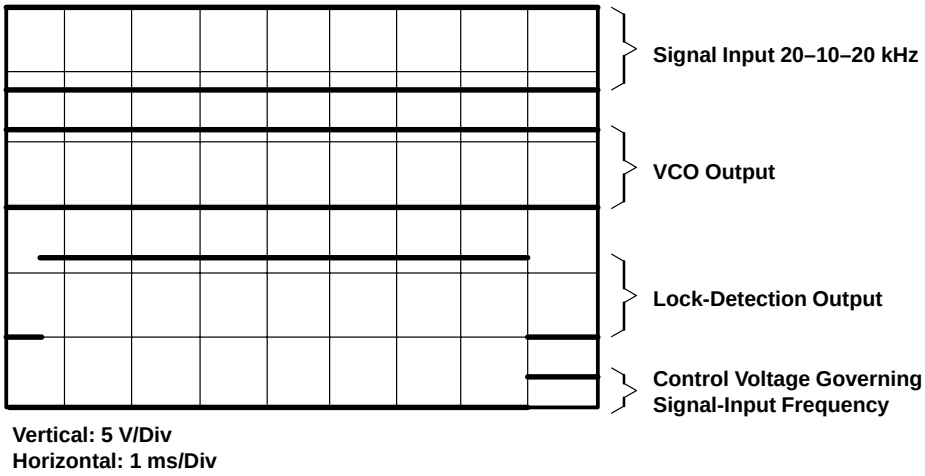

Figure 16. Lock-Detection-Circuit Waveforms

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