Experiment: Phase Locked Loop (PLL) - frequency synthesizer

1. Objectives

The objective of this experiment is to investigate the principles of Phase Locked Loop (PLL). The experiment consists in designing, putting into operation and measuring the frequency PLL synthesizer performances. The circuit is based ot the CMOS chip 4046, and two dividers 4520 and 4518.

2. Components and instrumentation

Block diagram of PLL (Phase Locked-Loop) is shown in Fig.1. The operation principle can be reduced to the control system, which maintains the local oscillator frequency so that both phase detector input frequencies are equal and the phase shift of these signals remains constant.

Schematic diagram of the circuit has been shown in Fig.2. Transistor Q1 matches the parameters of the signal generator used in the lab to the CMOS standard. The signal from the transistor is fed to the counter/divider K (Fig. 1) composed of the half of decade counter 4520 and half of the binary counter 4518. The total range of counter K can be selected from 4 to 160. The selection of the division is possible by means of jumpers Z1 and Z2. Frequency signal f_{in}/K is connected to the input phase detector (pin 14 of U3). Output of VCO 4046 is fed to the frequency divider N composed of the remaining halves of 4520 and 4518 systems and connected to the second input (pin 3) phase detector. The division ratio of N is determined by jumpers Z3 and Z4. Phase detector outputs (in the system are two different detectors) are connected with a jumper J1 to the low-pass filter and then to the VCO control inputs. Using the J1 Jumper, one can switch the type of phase detector used.

Resistors R1 and R2 and capacitor C1 determine the tuning range of the VCO. Resistors R3, R4 and capacitor C2 form a low-pass filter. Design rules for low pass filter are described in a data sheet of the 4046 IC.

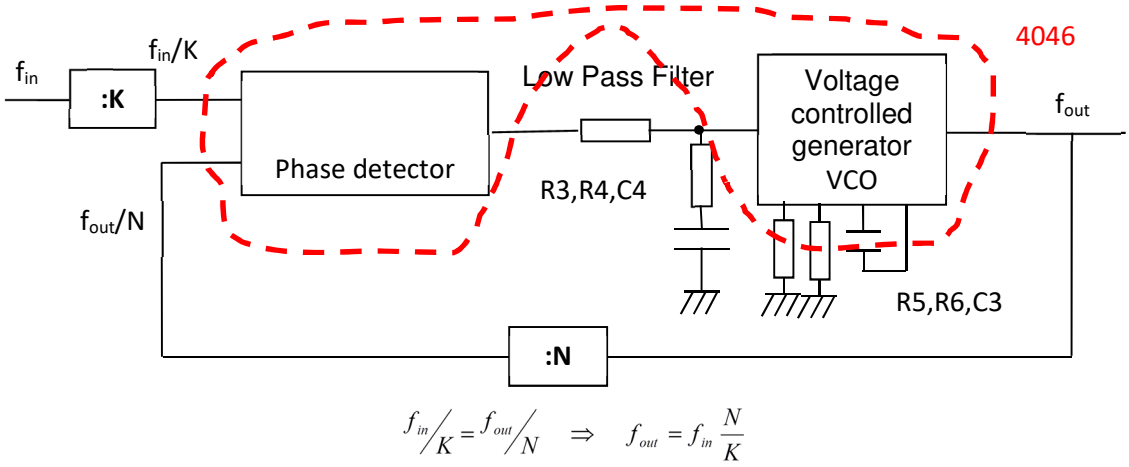

Fig.1. The principle of operation of the system frequency synthesizer

3. Preparation

Estimated time to prepare for classes is 2 to 6 hours.

3.1. Readings

1. Lecture notes ("PLL").
2. W. Tietze, Ch. Schenk, Electronic circuits – Handbook for Design and Applications, Spriger, 2008. Chapter 22.4
3. Data sheets and application notes of CMOS IC 4046, 4518 i 4520.

3.2. Problems

1. The principle of operation of a PLL,
2. The capture and lock frequency of a PLL.
3. The principle of operation of phase detectors implemented in IC 4046
4. Other phase detectors operation principle
5. Voltage Control Oscillator - examples and operating principle
6. The role of a low-pass filter
7. Application off PLL system (frequency synthesizer, AM, FM and PM demodulators)

3.3. Detailed preparation

1. Select the resistors R1, R2 and capacitor C1 to obtain the central frequency of the VCO of f0 = ... kHz and a tuning range Δf = ± ... ... kHz for a supply voltage Ucc = ... V
2. Choose low-pass filter components to achieve a range of capture Δfc = ± ... ... kHz (for type I phase detector)
3. The results of calculations put on the assembly diagram (Fig. 3)

If parameters in previous points are not specified by your tutor, chose parameters from the table right for Your group:

Group	f0 [kHz]	$2f_L$ [kHz]	$2f_C$ [kHz] (Phase det. I)	Ucc [V]
1 and 7	50	10	5	5
2, 8	70	15	7	8
3, 9	90	20	10	9
4, 10	100	25	15	10
5, 11	120	30	15	12
6, 12	150	35	15	15

4. Content of report

4.1. Assembling the circuit

Assemble the system. Plug in the power supply and the signal generator, the frequency counters to the input and the output of the system respectively. Check signals of the input transistor in a wide range of frequencies by observing the course of the collector voltage. The observed amplitude of the signal should be in range of few volts - TTL output generator can be used.

4.2. Measurement

1. Observe voltage waveforms on divider N and K outputs,
2. Measure tuning range of VCO by applying supply voltage and ground middle pin J2 junction.
3. Measure lock and capture frequency range for ratio N/K= 1, 2.5, 4, 5 and for both chase detectors (changed by J2 position)
   Synchronization can be detected by observing wave form in test points P3 and P4; they are signals on inputs of phase comparator – synchronization can be recognize as the moment when both waves stop;
4. Observe synchronization on harmonic frequency (for both phase detectors) .
5. Applying frequency modulated generator observe frequency detection using PLL.

Final report should contain:

a. Detailed calculation of the task of chapter 3.3 (obligatory) and computer simulation (optional)
b. Tabularized results of measurements ,
c. Oscilloscope prints of observed wave forms,
d. Conclusions of every point of chapter 4.2.

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				Tuning range of VCO f_{min}=…… kHz f_{max}=…… kHz							
				Phase det. I				Phase det. II			
N	K	N/K		$f_{LowLock}$ [kHz]	f_{LowCap} [kHz]	$f_{HighCap}$ [kHz]	$f_{HighLock}$ [kHz]	$f_{LowLock}$ [kHz]	f_{LowCap} [kHz]	$f_{HighCap}$ [kHz]	$f_{HighLock}$ [kHz]
			f_{in}								
			f_{out}								
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5. Appendixes

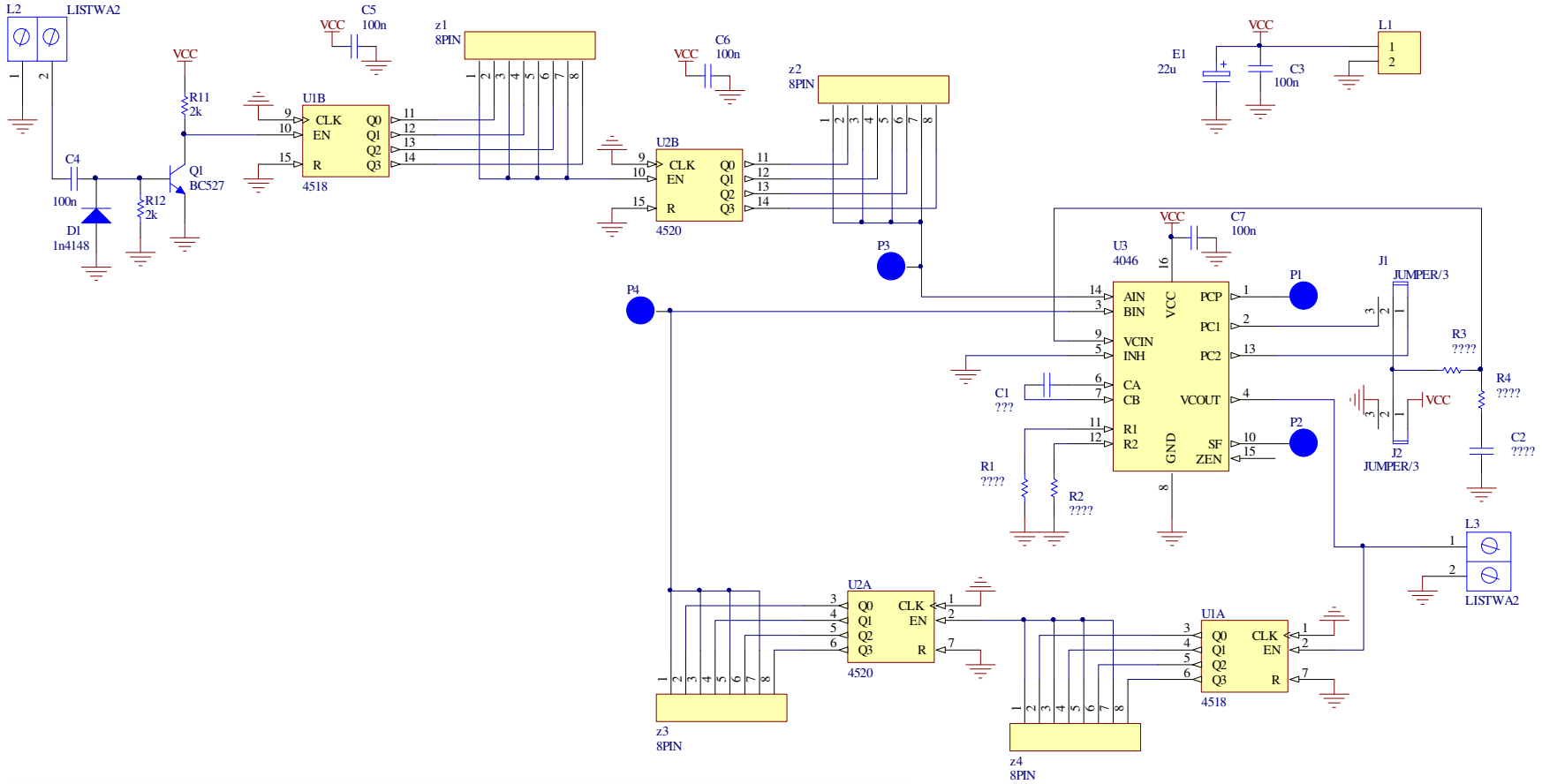

Fig.2. Schematic diagram of the system frequency synthesizer PLL

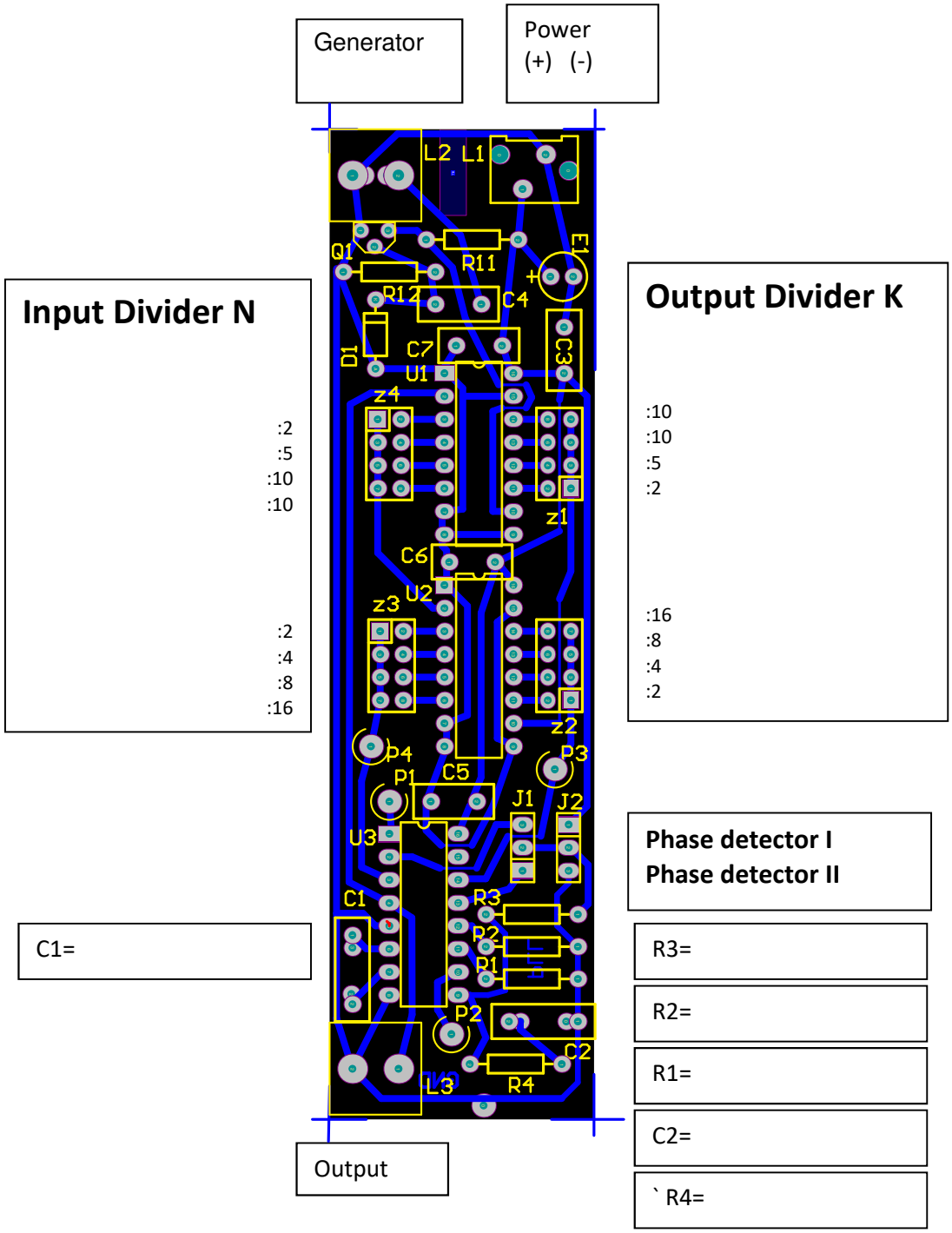

Fig.3. PCB of the frequency synthesizer PLL