Phase Locked-Loop

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Rferences

- U. Tietze, Ch.Schenk, Electronics Circuits – Handbook for Design and Applications, Springer,2008

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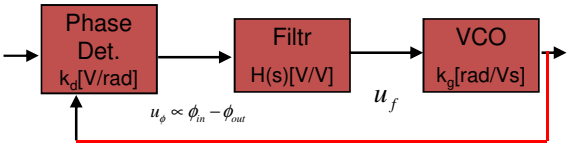
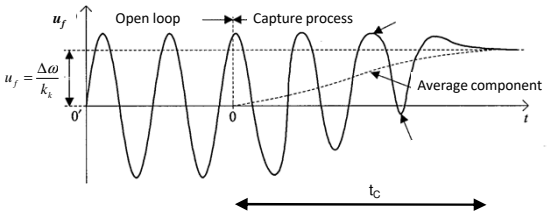
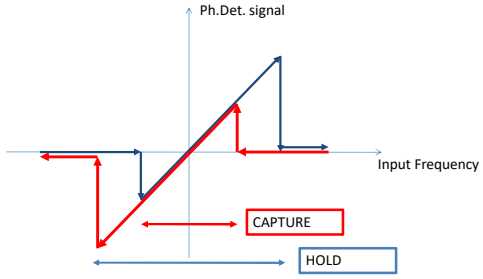
Phase-Locked Loop



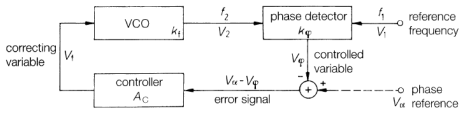
PLL synchronization process



PLL capture and hold frequency



Phase-Locked Loop



Principle of the phase-locked loop (PLL)

Phase-Locked Loop

$$\alpha - \varphi = \frac{f_1 - f_0}{Ac\, k_f\, k_\varphi} \qquad \alpha = \frac{V_\alpha}{k_\varphi} = -\varphi$$

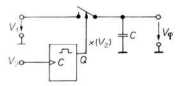
$$\varphi = \int_0^t \omega_2 d\tilde{t} - \int_0^t \omega_1 d\tilde{t} = \int_0^t \Delta\omega d\tilde{t} \qquad \Delta\omega(t) = \Delta\omega \cos\omega_m t$$

$$\varphi(t) = \frac{\Delta\omega}{\omega_m} \sin\omega_m t \qquad \frac{\varphi}{\Delta\omega} = \frac{1}{j\omega_m}$$

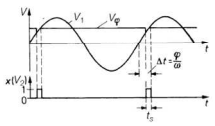
$$As = \frac{V_\varphi}{V_f} = \frac{2\pi k_f\, k_\varphi}{j\omega_m} = \frac{k_f\, k_\varphi}{jf_m}$$

Phase-Locked Loop

Sample-and-Hold Circuit as a Phase Detector



A sample-and-hold circuit used as a phase detector



Voltage weveform in the phase detector

PLL – SH as Ph.Det. - dynamics

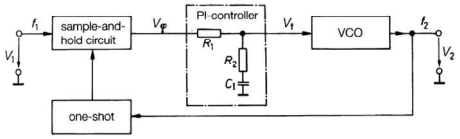
$$V_\varphi = \hat{V}_1 \sin\varphi \qquad V_\varphi \approx \hat{V}_1 \varphi / rad$$

$$k_\varphi = \frac{dV_\varphi}{d\varphi} = \hat{V}_1 / rad$$

$$k_\varphi = k_\varphi e^{-j\omega_m \frac{1}{2}T_2} = V_1 e^{-j\pi f_m / f_2} \qquad As = \frac{k_f k_\varphi}{jf_m} = \frac{k_f \hat{V}_1}{jf_m e^{j\pi f_m / f_2}}$$

$$As = \frac{|V_\varphi|}{|V_f|} = \frac{k_f \hat{V}_1}{f_m} \quad and \quad \varphi_m = -\frac{\pi}{2} - \frac{\pi f_m}{f_2}$$

PLL – SH as Ph.Det. - parameters

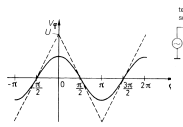


PLL with a sample-and-hold circuit as phase detector

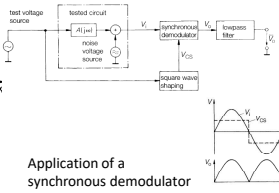
$$Ap = \frac{R_2}{R_1 + R_2}; \quad f_l = \frac{1}{2\pi C_1 R_2}; \quad A_l = 1$$

Phase-Locked Loop

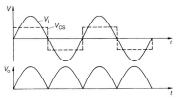
Sample-and-Hold Circuit as a Phase Detector



Mean absolute value of the output voltage of a multiplier for simusoidal input voltages of amplitude U



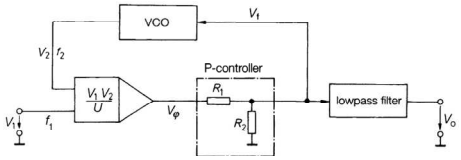
Application of a synchronous demodulator for the measurement of noisy signals



Operation of a synchronous demodulator

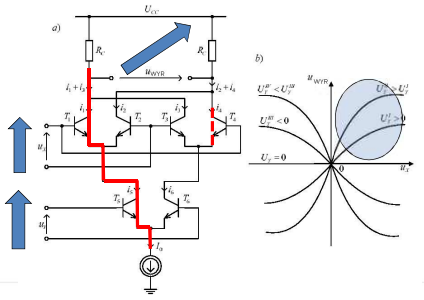
Phase-Locked Loop

Synchronous Detector as a Phase Detector



PLL with a multiplier as phase detector for frequency demodulation

Transconductance multiplier as a switch



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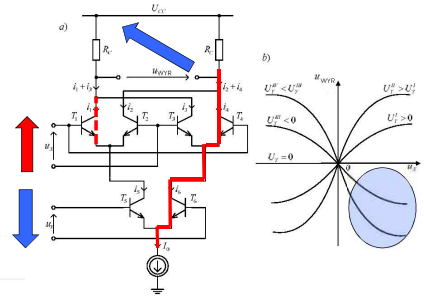
Transconductance multiplier as a switch



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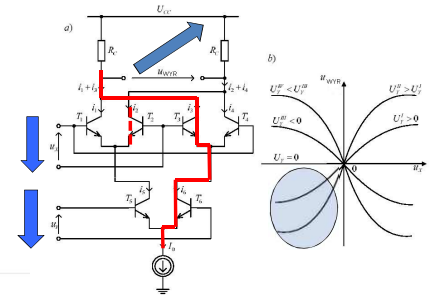
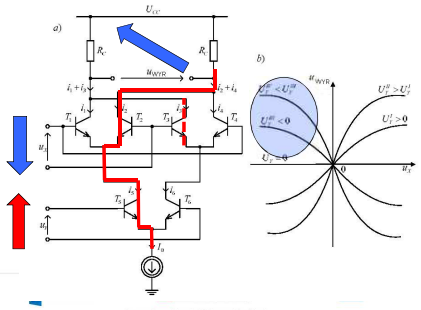
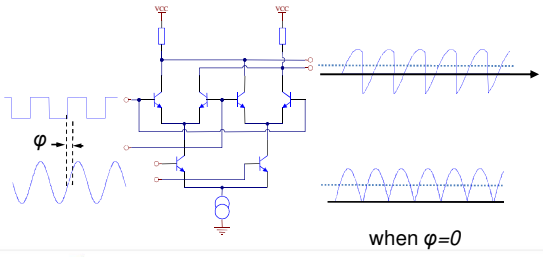
Transconductance multiplier as a switch



Transconductance multiplier as a switch



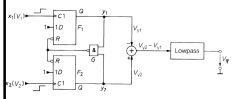
Multiplying circuit



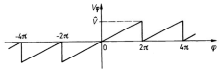
when $\varphi=0$

Phase-Locked Loop

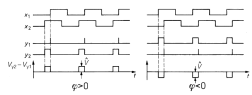
Frequency-Sensitive Phase Detector



Phase detector with memory for sign of the phase shift



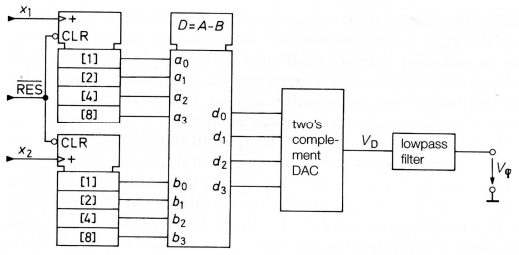
Transfer characteristic of the phase frequency detector



Input and output signals of the phase detector

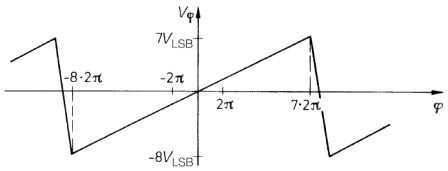
Phase-Locked Loop

Phase Detector with Extensive Range



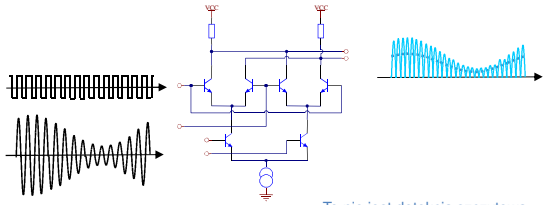
Phase-Locked Loop

Phase Detector with Extensive Range



Detection characteristic of the phase detector

Synchronous AM detector



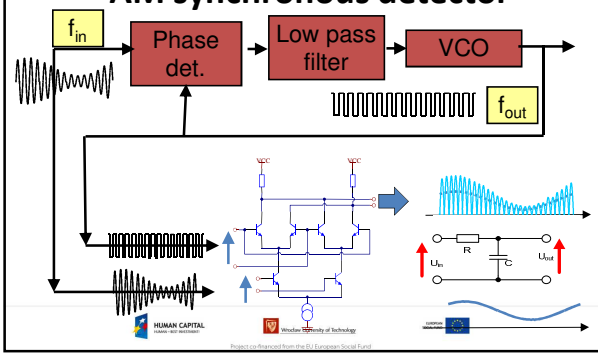
Gdy $\varphi=0$

To nie jest detekcja szczytowa, a średnia

PLL applications

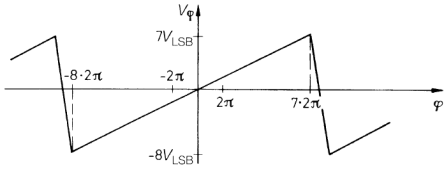
- AM demodulation
- Modulation and demodulation of FM i PM
- Frequency synthesis
- Synchronous detection (reference clock regeneration)
- Telecommunication (clock regeneration)

AM synchronous detector



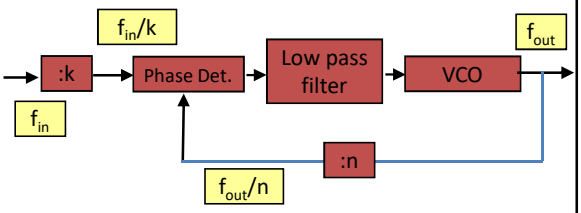
Phase-Locked Loop

Phase Detector with Extensive Range



Detection characteristic of the phase detector

Frequency synthesis



$$\frac{f_{in}}{k} = \frac{f_{out}}{n} \quad \Rightarrow \quad f_{out} = \frac{n}{k} f_{in}$$

Phase-Locked Loop

Sample-and-Hold Circuit as a Phase Detector

Type	Manufacturer	Technology	Frequency max	Principle
Phase detectors, PD				
AD 8343	Analog D.	Bipolar	2500 MHz	analog multiplier
AD 9100	Analog D.	Bipolar	200 MHz	sample-hold
AD 9901	Analog D.	TTL/ECL	200 MHz	phase/frequ. det.
MAX 9382	Maxim	PECL	450 MHz	phase/frequ. det.
LF 398	National	Bifet	0.3 MHz	sample-hold
MC 100EP 140	On Semi.	ECL	2000 MHz	phase/frequ. det
Voltage-controlled oscillators, VCOs				
F 100	Fujitsu	CMOS	30 MHz	piezo-oscillator
VC 80	Fujitsu	Bipolar	2500 MHz	LC-oscillator
LTC 1799	Lin. Tech.	CMOS	33 MHz	multivibrator
LTC 6905	Lin. Tech.	CMOS	170 MHz	multivibrator
MAX 2609	Maxim	PECL	600 MHz	LC-oscillator
MAX 2754	Maxim	Bipolar	1200 MHz	LC-oscillator
MC 100 EL 1648	On Semi.	ECL	1100 MHz	LC-oscillator
74 LS624	Texas I.	TTL	20 MHz	Multivibrator
VFC 110	Texas I.	Bipolar	4 MHz	V → f converter

Phase-Locked Loop

Sample-and-Hold Circuit as a Phase Detector

Type	Manufacturer	Technology	Frequency max	Principle
Phase-locked loops, PLLs				
74 HC 4046	many	CMOS	20 MHz	PD+VCO
AD 800	Analog D.	ECL	155 MHz	PD+VCO
AD 9540	Analog D.	PECL	655 MHz	PD+DDS+divider
CY 22394	Cypress	PECL/CMOS	400 MHz	PD+VCO+divider
CY 7B9940	Cypress	LVTTL	200 MHz	PD+VCO+divider
MPC 9331	Freescale	CMOS	240 MHz	PD+VCO+divider
ispclock 5500	Lattice	LVTTL	320 MHz	PD+VCO+divider
LMX 2325	National	BiCMOS	2500 MHz	PD+VCO+divider
NBC 12430	On Semi.	PECL	800 MHz	PD+VCO+divider
TLC 2932	Texas I.	TTL	32 MHz	PD+VCO

PLL applications

- AM Demodulation
- Synchronous detection (LockIn Amp)
- FM, PM demodulation
- Frequency synthesis
- Synchronous telekommunication

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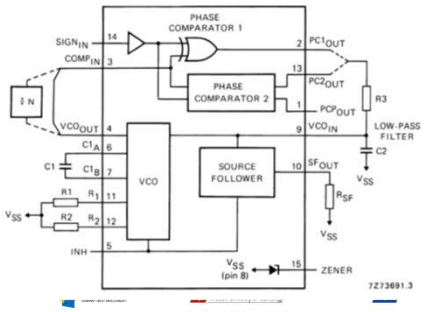
PLL IC - 4046



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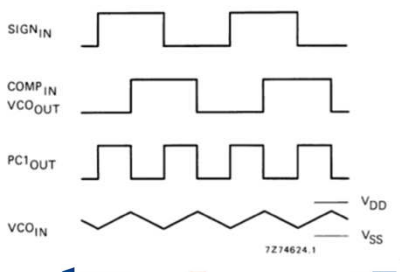
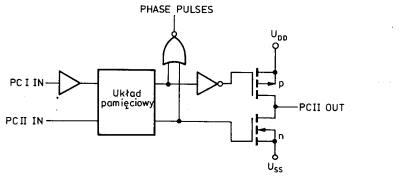
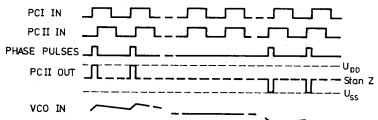
4046 phase detector I



4046 phase comparator II

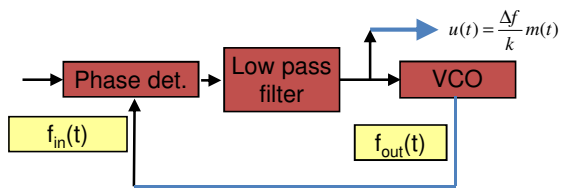




4046 features

Feature	Detector I (exor)	Detector II
Lack of input signal	$f_{wyj}=f_0$	$f_{wyj}=f_{min}$
Phase shift on output	90deg for f_0 0 to 180 in the range of $2f_T$	0deg
Harmonic synchronization	synchronize	No synchronization
Immunity t noise	high	low
$2f_T$ (lock range)	$f_{max} - f_{min}$	
$2f_c$ (capture range)	$f_C < f_T$ (depends on filter)	$f_C = f_T$

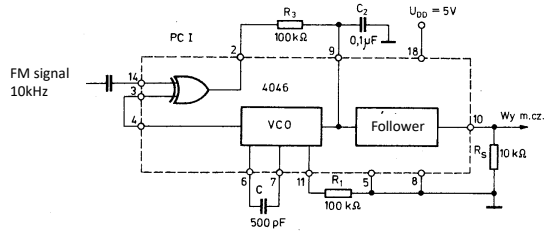
FM detector



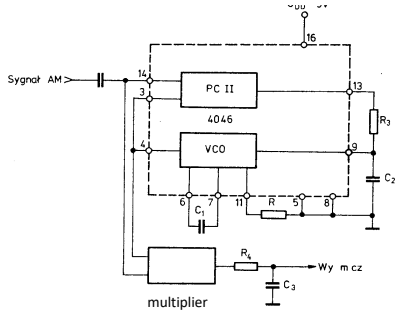
$$f_{in}(t) = f_0 + m(t) \cdot \Delta f$$
$$f_{out}(t) = f_0 + m(t) \cdot \Delta f$$
$$f_{out}(t) = f_0 + u(t) \cdot k$$

$$\Rightarrow \quad u(t) = \frac{\Delta f}{k} m(t)$$

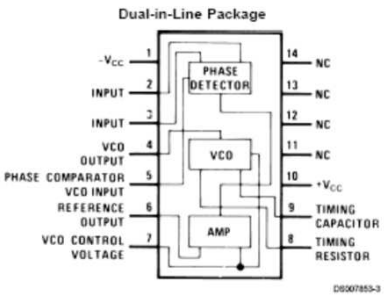
4046 as FM demodulator



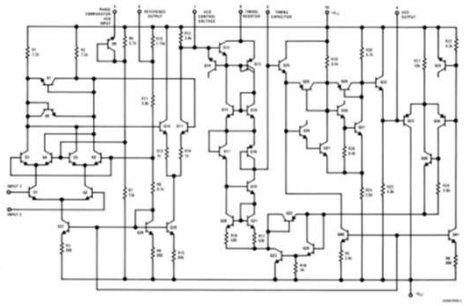
4046 as AM demodulator



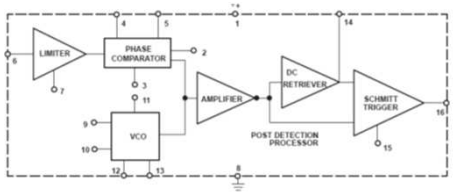
PLL IC LM565 (up to 500kHz)



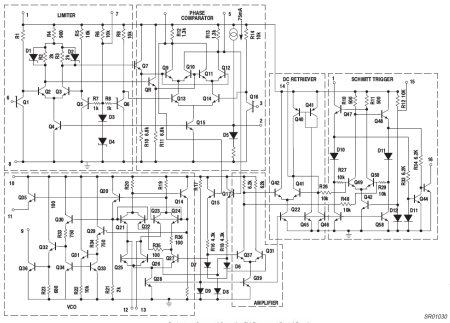
LM565



NE564



NE564 (up to 50MHz)



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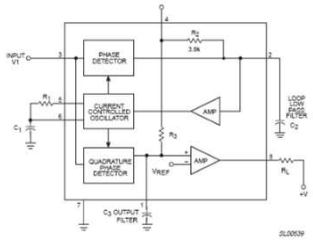
NE567



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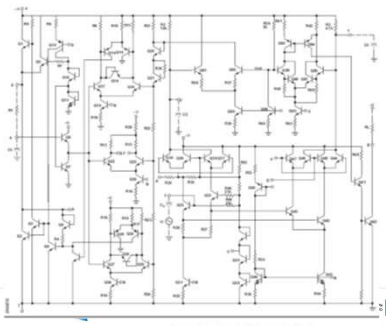

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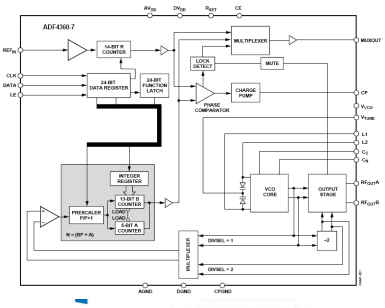
ADF4360-7
(350-1800MHz)



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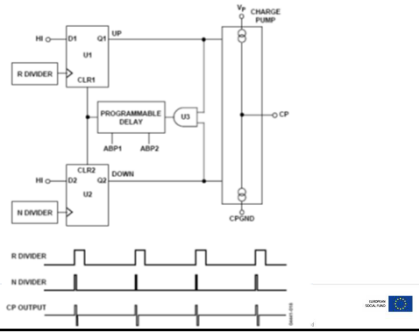
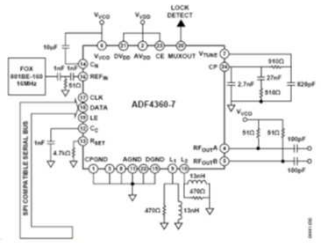
ADF4360-7 (350-1800MHz)



ADF4360-7 generator 500MHz



Summary

- PLL
  - Principle of operation
  - examples of VCO, filters, phase detectors
  - Applications – frequency synthesis, detectors

test questions

- What is the principle of operation of PLL ?
- What is the principle of operation of PLL as FM detector ?
- What is the principle of operation of PLL as AM synchronous detector ?
- What is the principle of operation of PLL as frequency synthesizer ?

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