


Phase Locked-Loop

Choose yourself and new technologies






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References


- U. Tietze, Ch.Schenk, Electronics Circuits – Handbook for Design and Applications, Springer, 2008

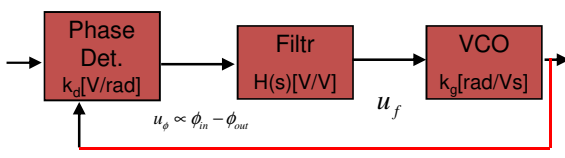
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Phase-Locked Loop



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PLL synchronization process

The graph shows the synchronization process of a PLL. The vertical axis is labeled u_f and the horizontal axis is labeled t . A sinusoidal wave represents the open loop signal. A dashed line represents the average component of the signal. The initial phase error is labeled $u_f = \frac{\Delta\omega}{k_f}$. The time taken for the signal to lock is labeled t_c . The process is divided into an "Open loop" phase and a "Capture process" phase.

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PLL capture and hold frequency

The graph plots the PLL's response to input frequency. The vertical axis is labeled "Ph.Det. signal" and the horizontal axis is labeled "Input Frequency". A red line shows the capture range, and a blue line shows the hold range. A red box labeled "CAPTURE" and a blue box labeled "HOLD" indicate the respective frequency ranges.

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Phase-Locked Loop

The block diagram illustrates the principle of a PLL. It consists of a VCO (Voltage-Controlled Oscillator) with gain K_v and a phase detector with gain K_ϕ . The VCO output is f_2 and V_2 . The phase detector output is f_1 (reference frequency) and V_1 (reference). The error signal is $V_e = V_\alpha - V_\phi$. The error signal is processed by a controller A_c to produce a correcting variable V_1 . The controlled variable is V_ϕ .

Principle of the phase-locked loop (PLL)

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Phase-Locked Loop

$$\alpha - \varphi = \frac{f_1 - f_0}{Ac k_f k_\varphi} \quad \alpha = \frac{V_\alpha}{k_\varphi} = -\varphi$$

$$\varphi = \int_0^t \omega_2 d\tilde{t} - \int_0^t \omega_1 d\tilde{t} = \int_0^t \Delta\omega d\tilde{t} \quad \Delta\omega(t) = \Delta\omega \cos \omega_m t$$

$$\varphi(t) = \frac{\Delta\omega}{\omega_m} \sin \omega_m t \quad \frac{\varphi}{\Delta\omega} = \frac{1}{j\omega_m}$$

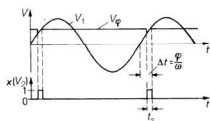
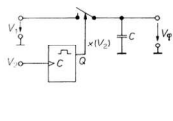
$$As = \frac{V_\varphi}{V_f} = \frac{2\pi k_f k_\varphi}{j\omega_m} = \frac{k_f k_\varphi}{jf_m}$$



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Phase-Locked Loop Sample-and-Hold Circuit as a Phase Detector



A sample-and-hold circuit used as a phase detector

Voltage waveform in the phase detector



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PLL – SH as Ph.Det. - dynamics

$$V_\varphi = \hat{V}_1 \sin \varphi \quad V_\varphi \approx \hat{V}_1 \varphi / \text{rad}$$

$$k_\varphi = \frac{dV_\varphi}{d\varphi} = \hat{V}_1 / \text{rad}$$

$$k_\varphi = k_\varphi e^{-j\omega_m \frac{1}{2} T_2} = V_1 e^{-j\pi f_m / f_2} \quad As = \frac{k_f k_\varphi}{jf_m} = \frac{k_f \hat{V}_1}{jf_m e^{j\pi f_m / f_2}}$$

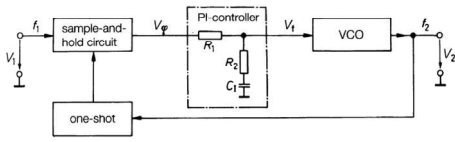
$$As = \frac{|V_\varphi|}{|V_f|} = \frac{k_f \hat{V}_1}{f_m} \quad \text{and} \quad \varphi_m = -\frac{\pi}{2} - \frac{\pi f_m}{f_2}$$



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PLL – SH as Ph.Det. - parameters



PLL with a sample-and-hold circuit as phase detector

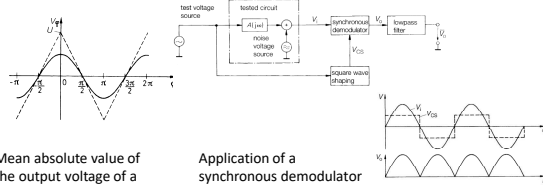
$$A_p = \frac{R_2}{R_1 + R_2}; \quad f_l = \frac{1}{2\pi C_1 R_2}; \quad A_f = 1$$



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Phase-Locked Loop Sample-and-Hold Circuit as a Phase Detector



Mean absolute value of the output voltage of a multiplier for sinusoidal input voltages of amplitude U

Application of a synchronous demodulator for the measurement of noisy signals

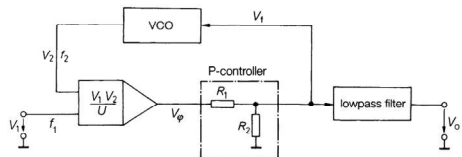
Operation of a synchronous demodulator



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Phase-Locked Loop Synchronous Detector as a Phase Detector



PLL with a multiplier as phase detector for frequency demodulation



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Transconductance multiplier as a switch

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Transconductance multiplier as a switch

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Transconductance multiplier as a switch

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Multiplying circuit

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Phase-Locked Loop Frequency-Sensitive Phase Detector

Phase detector with memory for sign of the phase shift

Input and output signals of the phase detector

Transfer characteristic of the phase frequency detector

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Phase-Locked Loop

Phase Detector with Extensive Range

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Phase-Locked Loop

Phase Detector with Extensive Range

Detection characteristic of the phase detector

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Synchronous AM detector

Gdy $\varphi=0$ To nie jest detekcja szczytowa,
a średnia

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PLL applications

- AM demodulation
- Modulation and demodulation of FM i PM
- Frequency synthesis
- Synchronous detection (reference clock regeneration)
- Telecommunication (clock regeneration)

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AM synchronous detector

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Phase-Locked Loop Phase Detector with Extensive Range

Detection characteristic of the phase detector

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Frequency synthesis

$$\frac{f_{in}}{k} = \frac{f_{out}}{n} \quad \Rightarrow \quad f_{out} = \frac{n}{k} f_{in}$$

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Phase-Locked Loop Sample-and-Hold Circuit as a Phase Detector

Type	Manufacturer	Technology	Frequency max	Principle
Phase detectors, PD				
AD8343	Analog D.	Bipolar	2500 MHz	analog multiplier
AD9100	Analog D.	Bipolar	200 MHz	sample-and-hold
AD9801	Analog D.	TTL/PECL	700 MHz	phase/frequ. det.
MAX9382	Maxim	PECL	450 MHz	phase/frequ. det.
LF398	National	Bifet	0.3 MHz	sample-and-hold
MC100EP140	On Semi.	ECL	2000 MHz	phase/frequ. det.
Voltage-controlled oscillators, VCOs				
F108	Fujitsu	CMOS	30 MHz	piezo-oscillator
VC80	Fujitsu	Bipolar	2500 MHz	LC-oscillator
LTC1799	Lin. Tech.	CMOS	33 MHz	multivibrator
LTC6905	Lin. Tech.	CMOS	170 MHz	multivibrator
MAX2609	Maxim	PECL	600 MHz	LC-oscillator
MAX2754	Maxim	Bipolar	1200 MHz	LC-oscillator
MC100EL1648	On Semi.	ECL	1100 MHz	LC-oscillator
74LS624	Texas I.	TTL	20 MHz	Multivibrator
VFC110	Texas I.	Bipolar	4 MHz	V → f converter

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Phase-Locked Loop Sample-and-Hold Circuit as a Phase Detector

Type	Manufacturer	Technology	Frequency max	Principle
Phase-locked loops, PLLs				
74HC4046	many	CMOS	20 MHz	PD+VCO
AD800	Analog D.	ECL	155 MHz	PD+VCO
AD9540	Analog D.	PECL	655 MHz	PD+DDS+divider
CY22394	Cypress	PECL/CMOS	400 MHz	PD+VCO+divider
CY7B9940	Cypress	LVTTTL	200 MHz	PD+VCO+divider
MPC9331	Freescale	CMOS	240 MHz	PD+VCO+divider
isplock5500	Lattice	LVTTTL	320 MHz	PD+VCO+divider
LMX2325	National	BiCMOS	2500 MHz	PD+VCO+divider
NBC12430	On Semi.	PECL	800 MHz	PD+VCO+divider
TLC2932	Texas I.	TTL	32 MHz	PD+VCO

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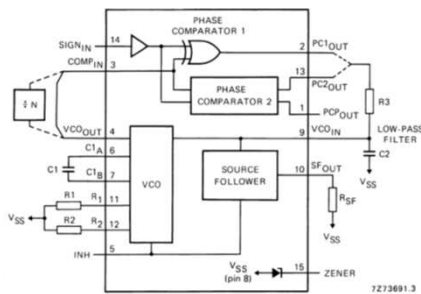
PLL applications

- AM Demodulation
- Synchronous detection (LockIn Amp)
- FM, PM demodulation
- Frequency synthesis
- Synchronous telecommunication



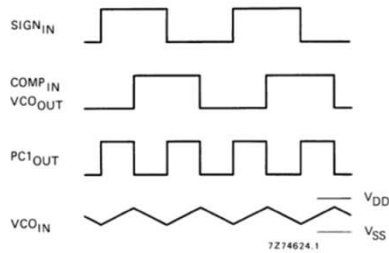


PLL IC - 4046





4046 phase detector I



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4046 phase comparator II

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4046 features

Feature	Detector I (exor)	Detector II
Lack of input signal	$f_{out} = f_0$	$f_{out} = f_{min}$
Phase shift on output	90deg for f_0 0 to 180 in the range of $2f_T$	0deg
Harmonic synchronization	synchronize	No synchronization
Immunity to noise	high	low
$2f_T$ (lock range)	$f_{max} - f_{min}$	
$2f_c$ (capture range)	$f_c < f_T$ (depends on filter)	$f_c = f_T$

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FM detector

$f_{in}(t) = f_0 + m(t) \cdot \Delta f$
 $f_{out}(t) = f_0 + m(t) \cdot \Delta f \implies u(t) = \frac{\Delta f}{k} m(t)$
 $f_{out}(t) = f_0 + u(t) \cdot k$

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4046 as FM demodulator

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4046 as AM demodulator

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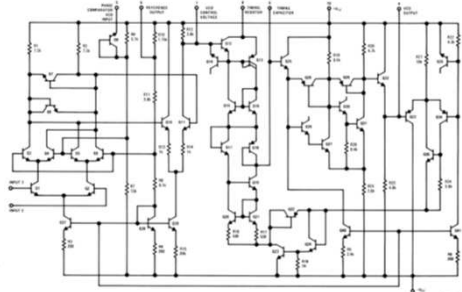
PLL IC LM565 (up to 500kHz)

D8007855-3

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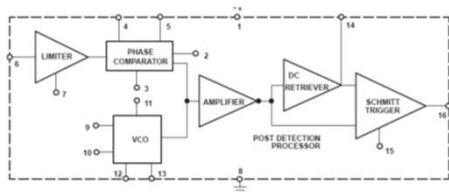
LM565



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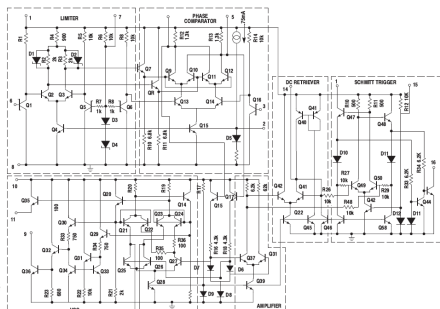
NE564



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NE564 (up to 50MHz)

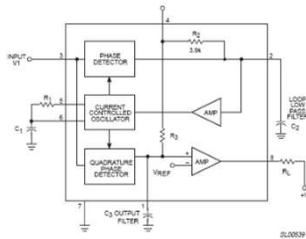


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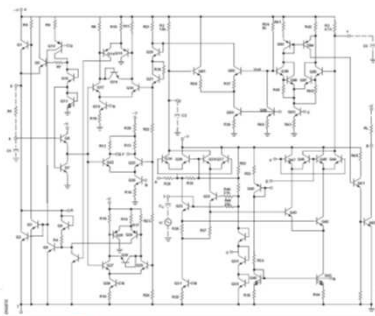
NE567



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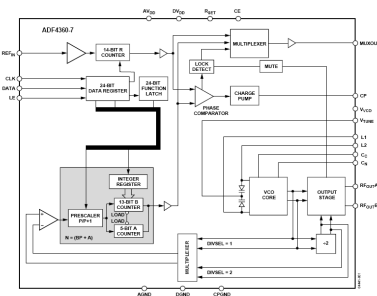
NE567



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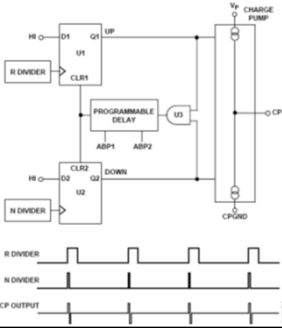
ADF4360-7 (350-1800MHz)



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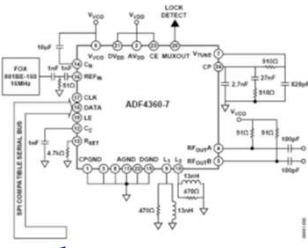


ADF4360-7 (350-1800MHz)





ADF4360-7 generator 500MHz





Summary

- PLL
 - Principle of operation
 - examples of VCO, filters, phase detectors
 - Applications – frequency synthesis, detectors



test questions

- What is the principle of operation of PLL ?
- What is the principle of operation of PLL as FM detector ?
- What is the principle of operation of PLL as AM synchronous detector ?
- What is the principle of operation of PLL as frequency synthesizer ?