

Analogue signals acquisition



My slides are subject to change without prior notice

Choose yourself and new technologies








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References

- U. Tietze, Ch.Schenk, Electronics Circuits – Handbook for Design and Applications, Springer, 2010
- Advertisement materials and Application notes of:
 - Linear Technology,
 - Analog Device,
 - Texas Instruments,
 - National Semiconductors
 - NEV Corporation








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Outline

- Acquisition system –general diagram
- ADC – general information
- Isolation methods
- Multiplexing problems
- Sample & hold – sampling frequency
- Widowing

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Intoduction

The intent of this and a few next lectures is to introduce the students to the most commonly used transducer interfaces and to provide practical information for dealing with the most frequently encountered transducers and their associated signals.

Transducers are available for measuring many physical quantities, such as temperature, pressure, strain, vibration, sound, humidity, flow, level, velocity, charge, pH, and chemical composition, among others. In most cases, the transducer manufacturer provides application notes on the transducer's use and principles of operation. The main questions to consider when selecting a transducer are:

- the electrical characteristics - source impedance, amplitude, frequency,
- power supply or excitation
- transducer's accuracy (taking frequency and range into account)
- calibration method
- verification of calibration
- environment of operation (temperature, humidity, vibration, pressure, etc.)

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General controll schematic outline

- impedance transformer
- amplifier
- multiplexer
- isolation

The diagram shows a control loop. On the left, a box labeled 'OBJECT UNDER CONTROL' and 'Physical environment' has an arrow pointing to a 'Front-end circuit'. This circuit is connected to an 'ADC' block. A vertical dashed red line labeled 'analogue isolation' separates the front-end circuit from the ADC. The ADC is connected to a 'computer' block. A vertical dashed red line labeled 'digital isolation' separates the ADC from the computer. The computer is connected to a 'PID controller' block. The PID controller is connected to a 'DAC' block. The DAC is connected to an 'actuator' block, which then has an arrow pointing back to the 'Physical environment'.

This elements can have different configuration !!!!

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ADC Analog to Digital Converters

- parallel converter – flash
- successive approximation
- pipeline
- voltage to frequency
- integrating converter (two, four slop)
- delta-sigma converter

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ADC – parallel (flash)

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2-step converter (direct, serial, pipeline)

Features (compared to „flash“):

- lower number comparators
- higher conversion time
- more popular (cheaper)
- higher resolution

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3-step converter (direct, serial, pipeline)

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ADC - successive approximation

Diagram illustrating the architecture of a successive approximation ADC. The input voltage V_{input} is compared against a DAC output. The comparator's output is used by the control logic and registers to iteratively adjust the DAC output until it matches the input voltage. The final digital output is then generated by the control logic and registers.

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ADC - voltage to frequency

Diagram illustrating the architecture of a voltage-to-frequency ADC. The input voltage V_{in} is converted into a digital pulse train by a voltage-to-frequency converter. This pulse train is then processed by a frequency meter, which includes timing circuitry and a pulse counter to produce digital outputs.

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ADC - integrating converter

Diagram illustrating the operation of an integrating converter. The capacitor voltage $V_{capacitor}$ increases linearly during the integration time T_i (where $I = V_{input}$) and then decreases linearly during the discharge time T_d (where a fixed discharge current is applied). The output voltage is given by the equation: $V_{output} = V_{ref} \cdot \frac{T_i}{T_d}$.

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Indirect converter ---four - slope

Phase	0	1	2	3	4
U_R	U_R	GND	U_R	U_i	U_R

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Four slope converter - „principle” of corrections

$$out = \frac{U_{REF}}{result(U_{REF}) - offset} \left(\frac{result - offset}{(1)} \right) =$$

$$= \frac{result - offset}{result(U_{REF}) - offset} U_{REF}$$

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„Σ-Δ” converter oversampling converter

for example 44,1 kHz 16 bit

for example 44,29 MHz

!!!!!!!
Sampling frequency f_{OSR} is much greater than reading frequency f_s

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„Σ-Δ” converter - principle of operation

The diagram shows four signals over time t :

- f_{OSR} : A high-frequency clock signal.
- V_i : An analog input signal.
- V_{AD} : A digital output signal (DAC output) that is a high-frequency square wave.
- V_{DA} : A digital-to-analog converter output signal that is a high-frequency square wave with a dashed line showing its average value following the input V_i .

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Oversampling „Σ-Δ” converter - general principle

The block diagram shows an input V_i entering a summing junction. The output of the summing junction goes to an integrator, then to an ADC (N bit). The ADC output V_{ADC} goes to a DAC (N bit), which outputs V_r back to the summing junction. The DAC output also goes to a decimation filter. The sampling frequency is $f_s = N \cdot f_{OSR}$. The final output is Z .

Samplig frequency	Resolution
f_{OSR}	N
$f_s \ll f_{OSR}$	N+x

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Noise shaping in „Σ-Δ” converter

Diagram A: Nyquist Operation. Shows a rectangular noise spectrum with a peak of $q/112$ (where $q = 1 \text{ LSB}$) from $f_s/2$ to f_s .

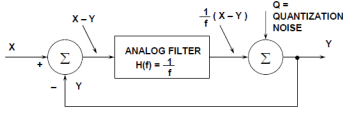
Diagram B: Oversampling + Digital Filter + Decimation. Shows a triangular noise spectrum with a peak of $Kf_s/2$ from $f_s/2$ to $Kf_s/2$. A digital filter removes noise above $f_s/2$.

Diagram C: Oversampling + Noise Shaping + Digital Filter + Decimation. Shows a triangular noise spectrum with a peak of $Kf_s/2$ from $f_s/2$ to $Kf_s/2$. A digital filter removes noise above $f_s/2$.

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„Σ-Δ” converter – linear model



$$Y = \frac{1}{f} (X - Y) + Q$$

REARRANGING, SOLVING FOR Y:

$$Y = \frac{X}{f+1} + \frac{Qf}{f+1}$$

SIGNAL TERM

NOISE TERM



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Conventional converter

$$U_{Nout} \propto \frac{1}{\sqrt{f_{os}/f_s}}$$

$$N_{bits} = \frac{20 \log \sqrt{f_{os}/f_s}}{6dB/bit}$$

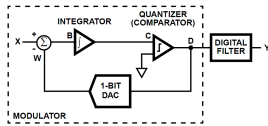
f_{os}/f_s	bit
2	0.5
4	1
256	4



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First order „Δ-Σ” converter



$$U_{Nout} \propto \left(\frac{1}{\sqrt{f_{os}/f_s}} \right)^3$$

$$N_{bits} = \frac{20 \log \left(\sqrt{f_{os}/f_s} \right)^3}{6dB/bit}$$

f_{os}/f_s	bit
2	1.5
4	3
256	12



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3rd order „Δ-Σ” converter

$$U_{\text{Noise}} \propto \left(\frac{1}{\sqrt{f_{os}/f_s}} \right)^5$$

$$N_{\text{bits}} = \frac{20 \log \left(\sqrt{f_{os}/f_s} \right)^5}{6 \text{dB/bit}}$$

f_{os}/f_s	bit
2	2.5
4	5
256	20

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Oversampling

number of bits (resolution): $N+6, N+5, N+4, N+3, N+2, N+1, N$

OSR = $\frac{f_{os}}{f_s}$

oversampling ratio

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Noise shaping in „Δ-Σ” converter

A Nyquist Operation

Quantization Noise = $q/112$
 $q = 1 \text{ LSB}$

B Oversampling + Digital Filter + Decimation

DIGITAL FILTER DEC

REMOVED NOISE

C Oversampling + Noise Shaping + Digital Filter + Decimation

ΣA MOD DIGITAL FILTER DEC

REMOVED NOISE

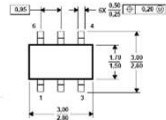
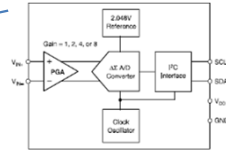
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Example of „ Δ - Σ ” converter ADS1110

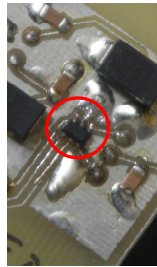
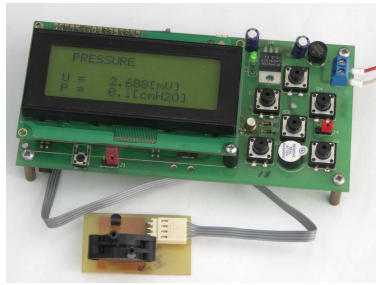
FEATURES

- COMPLETE DATA ACQUISITION SYSTEM IN A TINY SOT23-6 PACKAGE
- ONBOARD REFERENCE: Accuracy: 2.048V \pm 0.05% Drift: 5ppm/°C
- ONBOARD PGA
- ONBOARD OSCILLATOR
- 16-BITS NO MISSING CODES
- INL: 0.01% of FSR max
- CONTINUOUS SELF-CALIBRATION
- SINGLE-CYCLE CONVERSION
- PROGRAMMABLE DATA RATE: 16SPS TO 240SPS
- I²C INTERFACE—EIGHT AVAILABLE ADDRESSES
- POWER SUPPLY: 2.7V to 5.5V
- LOW CURRENT CONSUMPTION: 240 μ A



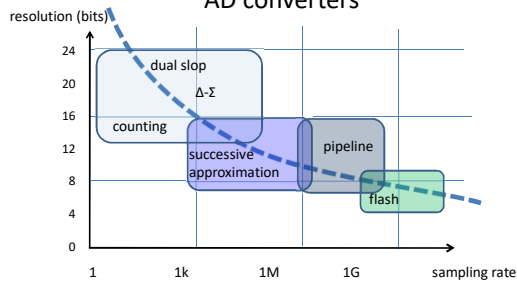


Lab setup of pressure sensor





General comparison of AD converters



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Resolution

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ADC – resolution and SNR

$$P_N = \int_{-\infty}^{\infty} x^2 p(x) dx = \frac{1}{\Delta} \int_{-\Delta/2}^{\Delta/2} x^2 dx = \frac{\Delta^2}{12} = \frac{(U_{FS}/2^n)^2}{12}$$

$$SNR = 10 \log \frac{P_S}{P_N} = 10 \log \left(\frac{(U_{FS}/2)^2}{\frac{(U_{FS}/2^n)^2}{12}} \right) = 6,02 \cdot n + 1,76 \text{ [dB]}$$

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ADC ----SNR

$$SNR = 10 \log \frac{P_S}{P_N} = 10 \log \left(\frac{(U_{FS}/2)^2}{\frac{(U_{FS}/2^n)^2}{12}} \right) = 6,02 \cdot n + 1,76 \text{ [dB]}$$

$SNR = 20 \log 2 = 6,02 \text{ [dB]}$

For every bit of resolution SNR increases by 6dB !!!!!!!

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For every bit of resolution, SNR increases by 6dB
 !!!!!!!!!

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Channel Capacity [bit / second]

$$CC[\text{bits/sec}] = f_{\text{samp}} n_{\text{bits}} = 2B \log_2 \left(\frac{U_{\text{amp}}}{\Delta U} \right) =$$

$$= 2B \frac{\log_{10} \left(\frac{U_{\text{amp}}}{\Delta U} \right)}{\log_{10}(2)} = 2B \frac{\left\{ 20 \log_{10} \left(\frac{U_{\text{amp}}}{\Delta U} \right) \right\}}{20 \log_{10}(2)} = B \frac{SNR}{10 \log_{10}(2)} = \frac{B \cdot SNR}{3}$$

$CC = \frac{B \cdot SNR}{3} [\text{bits/sec}]$

Shannon-Hartley theorem

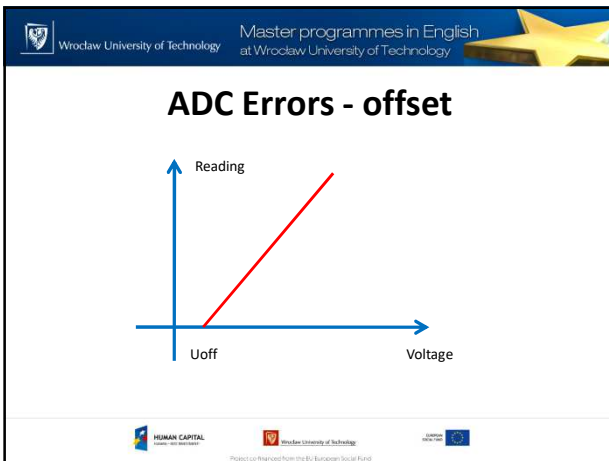
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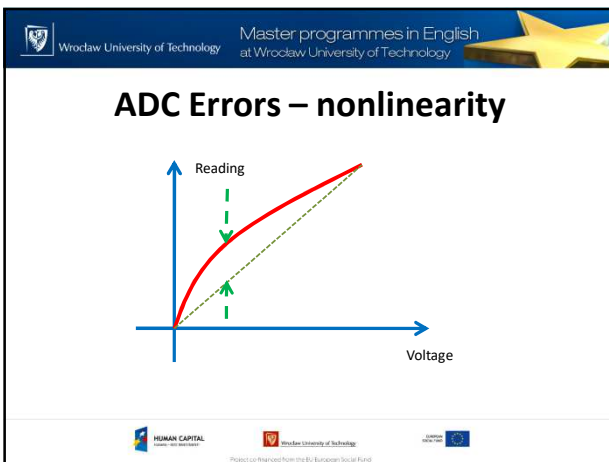
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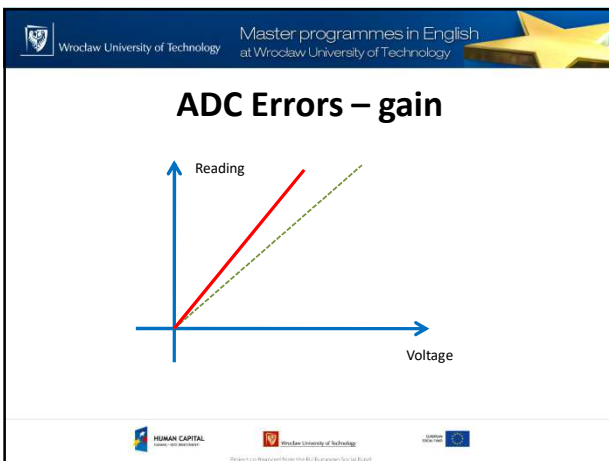
ADC Errors

- offset
- linearity
- gain
- missing codes
- noise (interferences)

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ADC Errors – missing codes

The graph plots 'Reading' on the vertical axis and 'Voltage' on the horizontal axis. A red line starts at the origin and increases linearly. At a certain voltage, the line becomes horizontal for a short interval, representing a missing code. After this interval, the line resumes its linear upward slope.

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ADC Errors - noise (interferences)

Controlling noise is first step to measure anything.

Spending money for accurate and high resolution ADC can be worthless when measuring signal is interfered by high level noise.

noise level should be smaller than resolution

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Digital to analog conversion

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Digital to Analogue Conversion

The parallel method: A ladder network of resistors \$R\$ and switches \$S_0, S_1, S_2, S_3\$ connected to \$V_{ref}\$ and ground. The output is \$V_O\$.

The weighting method: A network of resistors \$R, 2R, 4R, 8R\$ and switches \$z_0, z_1, z_2\$ connected to \$V_{ref}\$ and ground. The output is \$V_O\$.

Computing method: A single resistor \$R\$ and switch \$S\$ connected to \$V_{ref}\$ and ground. The output is \$V_O\$.

the parallel method the weighting method computing method

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Weighting conversion

A circuit diagram showing a reference voltage \$V_{ref}\$ connected to a series of resistors \$2R, 4R, 8R, 16R\$. Each resistor is connected to a switch \$z_3, z_2, z_1, z_0\$ respectively. The switches are connected to a common node \$I_k\$, which is the inverting input of an op-amp. The op-amp has a feedback resistor \$R_{FB}=R\$ and its non-inverting input is grounded. The output is \$V_O\$.

$$U_{out} = -U_{ref} \frac{N}{N_{max} + 1}$$

TIP:
difficult for manufacturing because of different R;
 U_{out} is loaded depending N;
stray capacitance of switches are charged or dis-
every change;

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Weighting conversion

A circuit diagram similar to the previous one, but with the resistors labeled \$2R, 4R, 8R, 16R\$ and switches \$z_3, z_2, z_1, z_0\$ labeled as MSB and LSB. The output is \$V_O\$.

$$U_{out} = -U_{ref} \frac{N}{N_{max} + 1}$$

TIP:
difficult for manufacturing because of different R;
 U_{out} is loaded depending N;
stray capacitance of switches are charged or dis-
every change;

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Ladder network

TIP:
 difficult for manufacturing because of different R;
 U_{out} is loaded depending N;
 stray capacitance of switches are charged or dis-
 every change;

$$U_{out} = -U_{ref} \frac{N}{N_{max} + 1}$$

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Ladder network converter without any amp

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Isolation

- Optical
- Magnetic
- Capacitive
- Analogue
- Digital

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„Digitaly” izolated analog signals

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Opto-Isolation of analog signals

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Analog opto-isolation

$$I_{PD1} = \frac{U_{in}}{R_1}$$

$$I_{PD2} = \eta I_{PD1}$$

$$I_{PD2} = \frac{U_{out}}{R_2}$$

$$U_{out} = U_{in} \frac{R_2}{R_1} \eta$$

Tip: accuracy can be is not satisfactory

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Opto-isolatin of 4-20mA loop

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PWM to 4-20mA isolation

LOOP POWERED PWM ISOLATED 4mA TO 20mA TRANSMITTER

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Magneto - Isolation

IL710

NVE corporation Advertisement materials

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Isolation by Pulse With Modulation (PWM)

(Burr Brown – advertisement materials)

The diagram shows an isolation barrier separating two op-amp stages, A1 and A2. Stage A1 is a non-inverting amplifier with a 200kΩ feedback resistor and a 150pF capacitor. Its input is connected to an input terminal V_{in} through a 200kΩ resistor. Stage A2 is an inverting amplifier with a 200kΩ feedback resistor and a 150pF capacitor. Its input is connected to an input terminal V_{in} through a 200kΩ resistor. Both stages have a 100μA current source. The output of A2 is V_{out}. An oscillator (Osc) provides a 100μA current source to the non-inverting input of A1. The circuit is powered by ±V_{cc} and GND 1/GND 2.

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Isolation by modulation

(Analog Device – advertisement materials)

The diagram shows the AD202 isolation module. It has an input section with IN+, IN-, and IN COM pins. The input signal is processed by a modulator (MOD) and a 25kHz oscillator. The modulated signal is transmitted through a transformer (25kHz) to a demodulator (DEM) section. The demodulator has HI and LO outputs and a V_{OUT} pin. The module is powered by a 15V DC supply through a power return pin. The power section includes a rectifier and filter (RECT AND FILTER) and an oscillator (OSCILLATOR). The module is powered by ±7.5V and ±5V FS supplies.

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Voltage-frequency modulation in transmission and isolation

The diagram illustrates voltage-frequency modulation in transmission and isolation. It shows a block labeled 'U/f' (voltage-to-frequency converter) connected to a 'long transmission line'. The signal is then processed by an 'isolator' block, which is connected to a 'Processor T/f acquisition' block. A blue arrow labeled 'fibre ISOLATION !!!' points from the U/f block to the processor, indicating the isolation mechanism.

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Multiplexing

- direct (small signal) multiplexing
- buffering – multiplexing
- simultaneous s/h
- digital multiplexing

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direct multiplexing

single ended or differential inputs

MUX

ADDRESS

GAIN !!
different for
different signals

ADC

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Input buffering

GAIN !! different for different signals

single ended or differential inputs

MUX

ADDRESS

GAIN !!
not necessary
!!!

ADC

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multiplexing with simultaneous reading

SAMPLING ADDRESS

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Switches to be continued during next lectures

$U_{CON}=VCC$
 $U_{COFF}=0$
 $R_{ON}<100\Omega$

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SH – sample and hold – basic circuit to be continued during next lectures

$R_{out}=0$ $R_{in}=\infty$

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Time acquisition channel

$$T_{sample} \geq \sqrt{T_1^2 + T_2^2} = T_{settle} \quad f_{acq} = \frac{1}{N_{channel} \cdot T_{sample}}$$

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Summary

- Acquisition system –general diagram
- ADC – general information
- isolation methods
- Multiplexing problems
- Sample & hold – sampling frequency

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Test questions (an example):

- In digital to analog conversion, what is the signal to quantization noise ratio ?
- What is the relationship between SNR and Channel Capacity ?
- Describe relationship between sampling ratio and resolution of AD converters.
- What are basic principles (methods) of galvanic isolation in analog and digital systems ?

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Multiplexers & switches – more about in „AD/DA converters lecture”

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Windowing (facultative)

[High- and moderate-resolution windows](#)

- [1 Rectangular window](#)
- [2 Hann window](#)
- [3 Hamming window](#)
- [4 Tukey window](#)
- [5 Cosine window](#)
- [6 Lanczos window](#)
- [7 Triangular windows](#)
- [8 Gaussian windows](#)
- [9 Bartlett–Hann window](#)
- [10 Blackman windows](#)
- [11 Kaiser windows](#)

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Windowing

[Low-resolution \(high-dynamic-range\) windows](#)

- [1 Nuttall window, continuous first derivative](#)
- [2 Blackman–Harris window](#)
- [3 Blackman–Nuttall window](#)
- [4 Flat top window](#)

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Windowing

[Other windows](#)

- 1 [Bessel window](#)
- 2 [Dolph-Chebyshev window](#)
- 3 [Hann-Poisson window](#)
- 4 [Exponential or Poisson window](#)
- 5 [Rife-Vincent window](#)
- 6 [DPSS or Slepian window](#)

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Main and side lobes

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Windowing rectangular window

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