Wroclaw University of Science and Technology

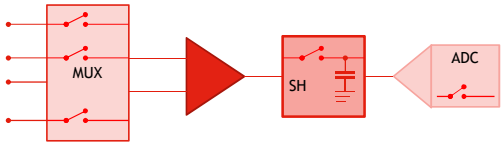
DA converters
Switches AND Sample&Hold

References

- U. Tietze, Ch.Schenk, Electronics Circuits – Handbook for Design and Applications, Springer

1. Analogue switches
2. Sample & Hold circuits (SH);(S/H)

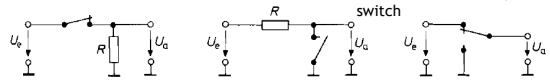
Measurement system and analogue switches



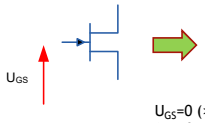
Switches - basic configurations

Basic features:
1. forword attenuation (ON resistance)
2. reverse attenuation (OFF resistance)
3. voltage range
4. switching time

Basic configurations:
a) series switch
b) short-circuing switch
c) series/short-circuiting switch



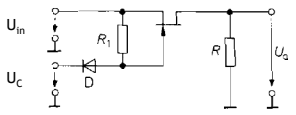
FET switches



U_{GS}=0 (>)
R_{ON}=few or fraction of Ω

U_{GS}<U_{th} (negative)
R_{OFF}=hundrets /thouseds of kΩ

FET series switch - driving circuit



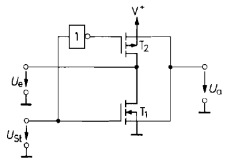
$U_{CON}=U_{inmax}$
$U_{COFF}<= U_{in}+U_{th}$ (must be negative)

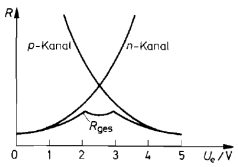
Mosfet switch

$U_{GS}>0$ (a few of Volts)
R_{ON}=few or fraction of Ω

$U_{GS}<=0$ (negative)
R_{OFF}=hudreds touseds of kΩ

Transmision gate (4066)





U_{CON}=VCC
U_{COFF}=0
R_{ON}<100Ω

MOSFET switches overview

Type	Manu-facturer	Function	On resistance	Voltage range	Power dissipation	Response time
Without level translator, unprotected						
74 HC 4016	Philips	4 × SPST	65 Ω	0…12 V	10 µW	10 ns
74 HC 4053	Philips	3 × SPDT	60 Ω	0…12 V	10 µW	20 ns
74 HC 4066	Philips	4 × SPST	35 Ω	0…12 V	10 µW	20 ns
MAX 4522	Maxim	4 × SPST	60 Ω	0…12 V	10 µW	10 ns
SD 5000	Vishay	4 × SPST	30 Ω	± 10 V	10 µW	1 ns
Fast switching (≤ 100 ns)						
HI 201 HS	Intersil	4 × SPST	30 Ω	± 15 V	120 mW	30 ns
74 HC 4316	Philips	4 × SPST	65 Ω	± 5 V	10 µW	20 ns
DG 611	Vishay	4 × SPST	18 Ω	± 5 V	20 µW	15 ns
Low power (≤ 100 µW) and low on resistance (≤ 100 Ω)						
ADG 511	Analog D.	4 × SPST	30 Ω	± 20 V	20 µW	200 ns
DG 403	Intersil	2 × SPDT	30 Ω	± 15 V	20 µW	150 ns
DG 411	Intersil	4 × SPST	30 Ω	± 15 V	30 µW	150 ns
LT 221	Lin. Tech.	4 × SPST	70 Ω	± 15 V	10 µW	250 ns
MAX 351	Maxim	4 × SPST	22 Ω	± 15 V	35 µW	150 ns
DG 405	Vishay	4 × SPST	20 Ω	± 15 V	10 µW	100 ns

MOSFET switches overview cont.

Low on resistance (≤ 100 Ω)						
ADG 211	Analog D.	4 × SPST	60 Ω	± 15 V	10 µW	200 ns
ADG 333	Analog D.	4 × SPDT	20 Ω	± 15 V	1 µW	150 ns
ADG 451	Analog D.	4 × SPST	5 Ω	± 15 V	20 µW	60 ns
MAX 4602	Maxim	4 × SPST	2 Ω	± 15 V	1 µW	180 ns
CDG 271	Vishay	4 × SPST	32 Ω	± 15 V	150 mW	50 ns
High voltage (≥ ± 30 V)						
HV 348	Supertex	2 × SPST	35 Ω	± 50 V	10 mW	500 ns
High off attenuation (≥ 40 dB @ 100 MHz)						
HI 222	Intersil	2 × SPST	35 Ω	± 15 V	75 mW	90 ns
MAX 4545	Maxim	2 × SPST	50 Ω	± 5 V	1 µW	100 ns
DG 540	Vishay	4 × SPST	30 Ω	± 6 V	60 mW	30 ns

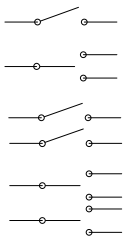
Understanding switches description

SPST

SPDT

DPST

DPDT



Single(Double)Pole

Single(Double;Triple)Throw

SPCO - centere off

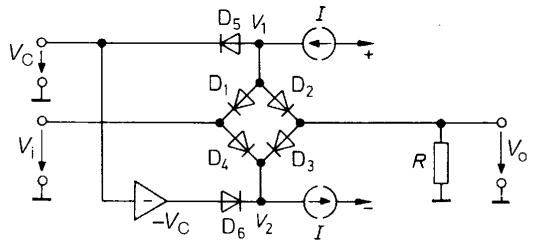
Analogue multiplexers

Type	Manu-facturer	Function	On resistance	Voltage range	Power dissipation	Response time	Data latch
Fast switching (≤ 100 ns), unprotected							
74 HC 4051	Philips	1 × 8	60 Ω	± 5 V	10 µW	20 ns	no
74 HC 4052	Philips	2 × 4	60 Ω	± 5 V	10 µW	20 ns	no
74 HC 4053	Philips	3 × 2	60 Ω	± 5 V	10 µW	20 ns	no
Low power (≤ 100 µW)							
DG 406	Maxim	1 × 16	80 Ω	± 15 V	20 µW	300 ns	no
DG 408	Maxim	1 × 8	80 Ω	± 15 V	20 µW	200 ns	no
DG 685	Vishay	1 × 8	55 Ω	± 15 V	10 µW	160 ns	yes
High input protection (≥ ±30 V)							
MAX 378	Maxim	1 × 8	2 kΩ	± 15 V	2 mW	300 ns	no
DG 458	Intersil	1 × 8	80 Ω	± 15 V	5 mW	200 ns	no
High voltage (≥ ± 30 V)							
HV 22816	Supertex	1 × 8	22 Ω	± 80 V	2 mW	4 µs	yes

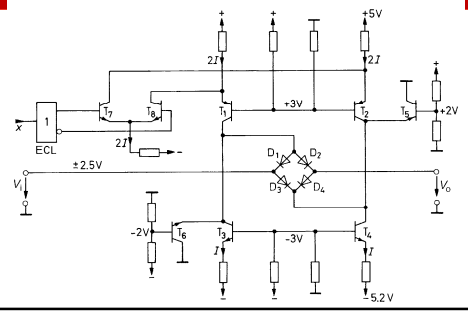
Analogue multiplexers cont.

High off attenuation (≥ 40 dB @ 100 MHz)							
MAX 310	Maxim	1 × 8	150 Ω	± 12 V	1 mW	300 ns	no
DG 536	Vishay	1 × 16	55 Ω	0…10 V	75 µW	200 ns	yes
DG 538	Vishay	2 × 4	45 Ω	± 6 V	10 mW	200 ns	yes
Universal types							
ADG 408	Analog D.	1 × 8	80 Ω	± 15 V	2 mW	200 ns	no
ADG 526	Analog D.	1 × 16	280 Ω	± 15 V	10 mW	200 ns	yes
DG 408	Intersil	1 × 8	80 Ω	± 15 V	7 mW	200 ns	no
MAX 308	Maxim	1 × 8	60 Ω	± 15 V	300 µW	200 ns	no

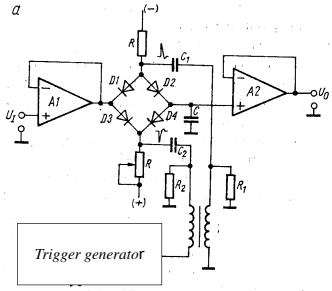
diode switches- a series switch



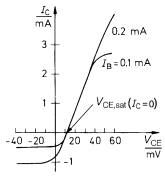
diode switches- an example of control circuit

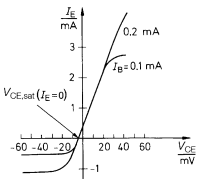


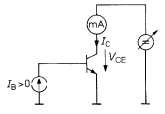
Sample & hold with diode switch

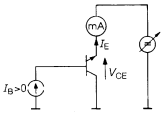


Bipolar transistor switch

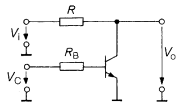


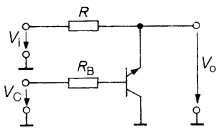






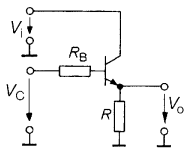
Short circuiting switch

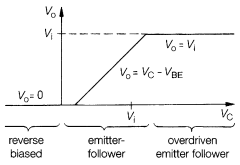




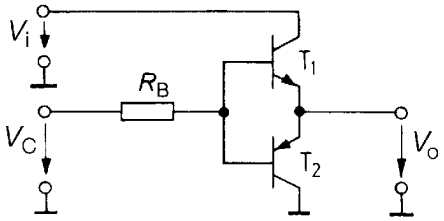
invert operation

Series (emiter folower) switch

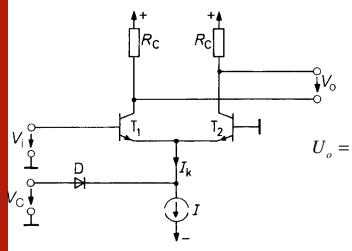




Series/short circuiting switch

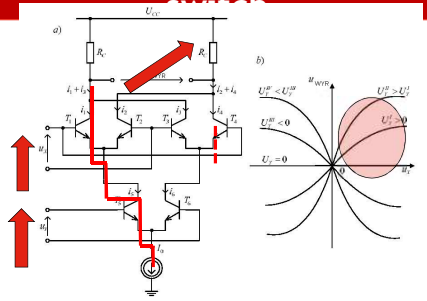


differential amp as switch

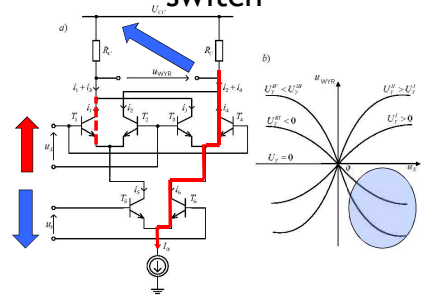


$$U_o = \begin{cases} 0 & U_C = +1V \\ g_m R_C U_i & U_C = -1V \end{cases}$$

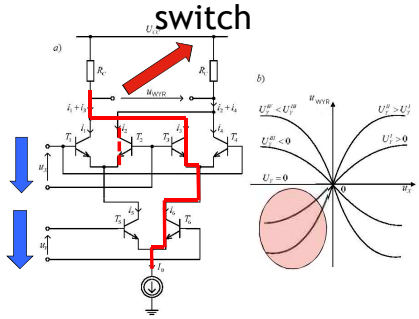
Transconductance multiplier as a switch



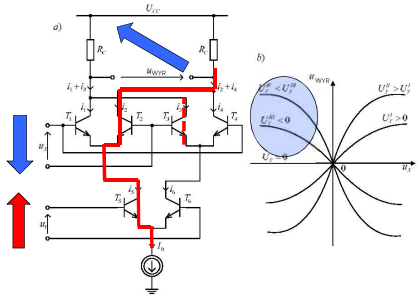
Transconductance multiplier as a switch



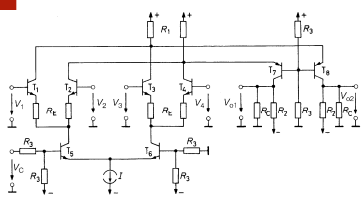
Transconductance multiplier as a switch



Transconductance multiplier as a switch

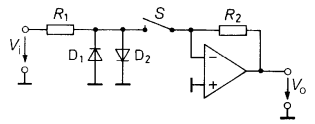


Switching of differential signals



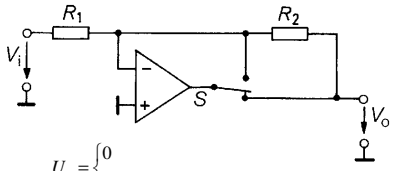
$$U_o = \begin{cases} A(U_1 - U_2) & U_C = +1V \quad A = \frac{1}{2} g_m^{'} (R_C \parallel R_2) \\ A(U_3 - U_4) & U_C = -1V \quad g_m^{'} = g_m / (1 + g_m R_E) \end{cases}$$

High voltage switch with „low voltage switch”



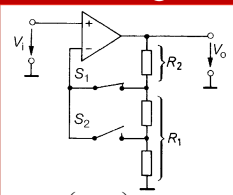
$$U_o = \begin{cases} 0 \\ -U_i R_2/(R_1 + r_{on}) \end{cases}$$

Precision high voltage switch

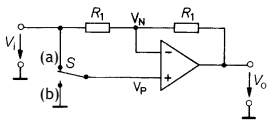


$$U_o = \begin{cases} 0 \\ -U_i R_2/R_1 \end{cases}$$

PGA Programable Gain Amplifier



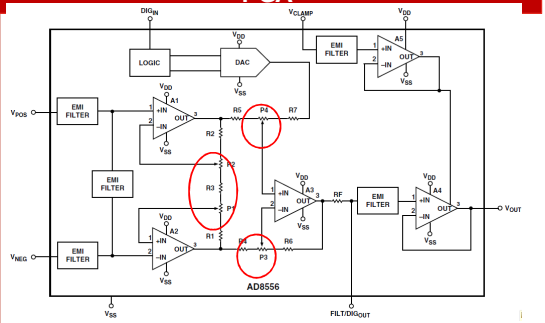
$$U_o = U_i\left(1 + \frac{R_2}{R_1}\right)$$



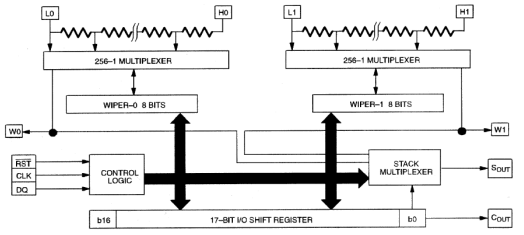
$$U_o = \begin{cases} +U_i & (a) \\ -U_i & (b) \end{cases}$$

TIP:gain is independent from switch ON resistance

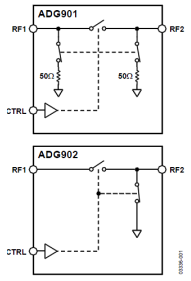
PGA



potetiometer inside



HF switches - GaAs MESFET

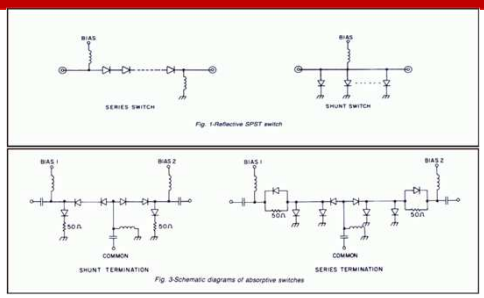


series/shunt

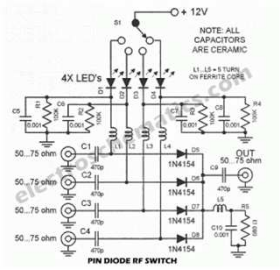
Absorptive

Reflective Switches

HF switches - PIN diode

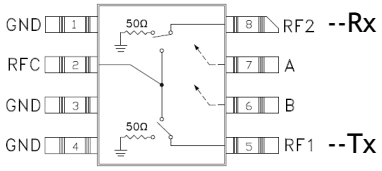


HF mux



RF switches with MESFET

Antenna--



--Rx

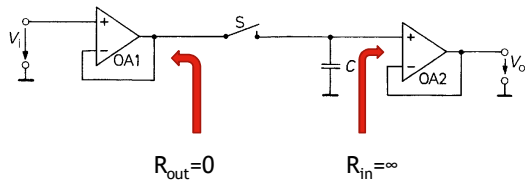
--Tx

non-reflective GaAs MESFET SPDT

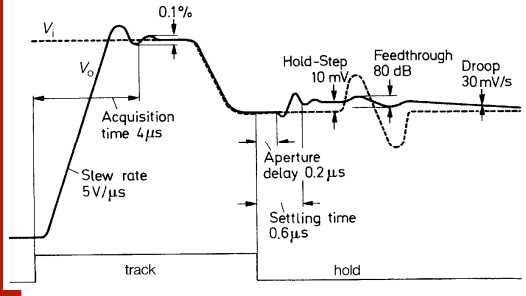
High Power switches
MOSFET IGBT

OUT OF TOPIC

SH - sample and hold - basic circuit



SH characteristic an example (LF398)



SH parameters

Aquisition time (capacitor SMALL)

$$t_{AC} = R_s C \cdot \begin{cases} 4.6 & 1\% \, of \, error \\ 6.9 & 0.1\% \, of \, error \end{cases}$$

Aperture delay (capacitor should be SMALL)
Aperture jitter
Hold step (capacitor should be LARGE)

$$\Delta U_o = \frac{C_s}{C} \Delta U_C$$

Setting time (capacitor should be SMALL)
Feedthrough (capacitor should be LARGE)
Droop (hold decay) (capacitor should be LARGE)

$$\Delta U_o = \frac{I_d}{C} \Delta t$$

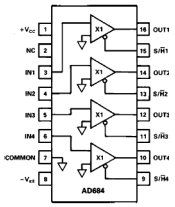
SH capacitor

Recommended:
teflon
polystyrene
polypropylene

Not recommended (leakage, charge storage)
polycarbonate
mylar
ceramic (definitely BAD)

AD 684 SH

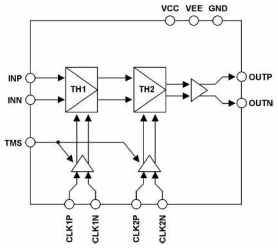
FEATURES
Four Matched Sample-and-Hold Amplifiers
Independent Inputs, Outputs and Control Pins
500 ns Hold Mode Settling
1 μs Maximum Acquisition Time to 0.01%
Low Droop Rate: 0.01 μV/μs
Internal Hold Capacitors
75 ps Maximum Aperture Jitter
Low Power Dissipation: 430 mW
0.3" Skinny DIP Package
MIL-STD-883 Compliant Versions Available

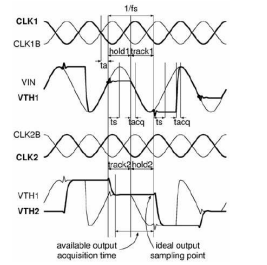


20 GHz Bandwidth High Linearity Track-and-Hold

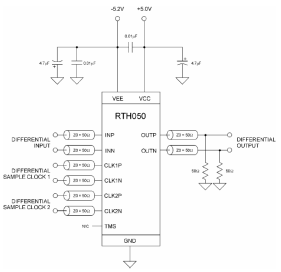
Features

- 15 GHz Small Signal Input Bandwidth
- 13 GHz Input Bandwidth (0.25 Vpp SE)
- 100 - 1000 MHz Sampling Rate (TH1)
- 10 - 1000 MHz Output Data Rate (TH2)
- -40 dB Hold Mode Distortion (4.0 GHz 0.25 Vpp SE V_{IN})
- -36 dB Hold Mode Distortion (4.0 GHz 0.25 Vpp SE V_{IN})
- < 100 fs Aperture Jitter
- < 200 ps Acquisition Time
- < 25 ps Rise Time (20 - 80%)
- Differential Analog Input/Output
- 1.6W Power Dissipation
- Output Held more than Half Clock Cycle
- Track Mode Select

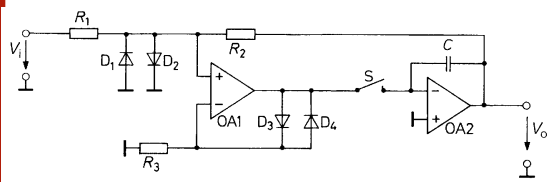




Timing diagram for out-of-phase clocking of TH1 and TH2



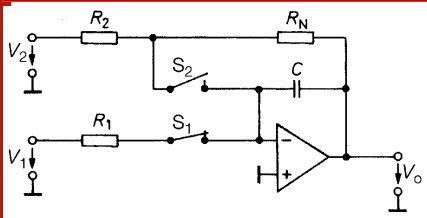
SH with an integrator



SH with an integrator

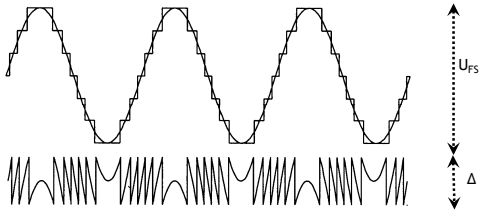
Type	Manu-facturer	Hold capacitor	Setting time	Accuracy	Slew rate	Droop	Tech-nology
LF 398	various	10 nF	20 µs	10 bit	0,5 V/µs	3 mV/s	Bifet
LF 398	**various**	**1 nF**	**4 µs**	**10 bit**	**5 V/µs**	**30 mV/s**	**Bifet**
AD 585	Analog Dev.	100 pF*	3 µs	12 bit	10 V/µs	0,1 V/s	Bipolar
SHC 5320	Burr Brown	100 pF*	1.5 µs	12 bit	45 V/µs	0,1 V/s	Bipolar
AD 781	**Analog Dev.**	*	**0.6 µs**	**12 bit**	**60 V/µs**	**10 mV/s**	**Bimos**
AD 682[2]	Analog Dev.	*	0.6 µs	12 bit	60 V/µs	10 mV/s	Bimos
AD 684[4]	Analog Dev.	*	0.6 µs	12 bit	60 V/µs	10 mV/s	Bimos
AD 783	**Analog Dev.**	*	**0.2 µs**	**12 bit**	**50 V/µs**	**20 mV/s**	**Bimos**
LF 6197	**National**	**10 pF***	**0.2 µs**	**12 bit**	**145 V/µs**	**0,6 V/s**	**Bifet**
AD 9100	**Analog Dev.**	**22 pF***	**16 ns**	**12 bit**	**850 V/µs**	**1 kV/s**	**Bipolar**
RTH 050	**Rockwell**	*	**0.2 ns**	**8 bit**	**40 kV/µs**		**GaAs**

SH with initial value

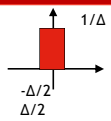


S1/S2 on/off - integration
S1/S2 off/on - initial value
S1/S2 off/off - hold

Resolution



ADC - resolution and SNR



$$P_N = \int_{-\infty}^{\infty} x^2 p(x)dx = \frac{1}{\Delta}\int_{-\Delta/2}^{\Delta/2} x^2 dx = \frac{\Delta^2}{12} = \frac{\left(U_{FS}/2^n\right)^2}{12}$$

$$SNR = 10\log\frac{P_S}{P_N} = 10\log\left(\frac{\frac{\left(U_{FS}/2\right)^2}{2}}{\frac{\left(U_{FS}/2^n\right)^2}{12}}\right) = 6{,}02\cdot n + 1{,}76 \quad [dB]$$

ADC ----SNR

$$SNR = 10\log\frac{P_S}{P_N} = 10\log\left(\frac{\frac{\left(U_{FS}/2\right)^2}{2}}{\frac{\left(U_{FS}/2^n\right)^2}{12}}\right) = 6{,}02\cdot n + 1{,}76 \quad [dB]$$

$$SNR = 10\log 2 = 6{,}02\,[dB]$$

For every bit resolution SNR increases of 6dB !!!!!!!!

For every bit of resolution the SNR increases of 6dB

!!!!!!!!

Channel Capacity [bit / second]

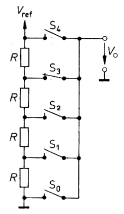
$$CC[bits/\sec] = f_{sampl} n_{bits} = 2B\log_2\left(\frac{U_{amp}}{\Delta U}\right) =$$

$$= 2B\frac{\log_{10}\left(\frac{U_{amp}}{\Delta U}\right)}{\log_{10}(2)} = 2B\frac{\left\{20\log_{10}\left(\frac{U_{amp}}{\Delta U}\right)\right\}}{20\log_{10}(2)} = B\frac{SNR}{10\log_{10}(2)} = \frac{B\cdot SNR}{3}$$

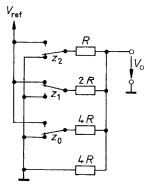
$$CC = \frac{B\cdot SNR}{3}[bits/\sec]$$

Shannon-Hartley theorem

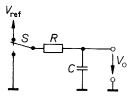
Digital to Analogue Conversion



the parallel method

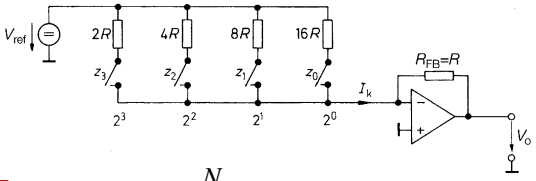


the weighting method



computing method

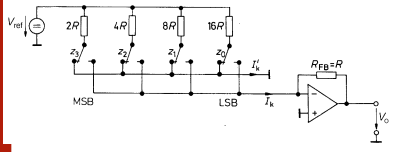
Weighting conversion



$$U_{out} = -U_{ref}\frac{N}{N_{max}+1}$$

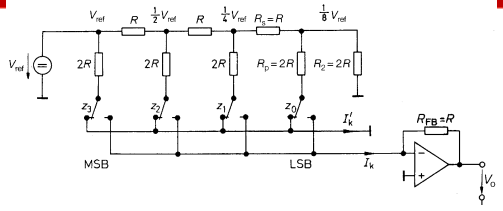
TIP:
difficult for manufacturing because of different R;
U_{ref} is loaded depending N;
stray capacitance of switches are charged or dis- every change;

Weighting conversion



TIP:
difficult for manufacturing because of different R;
~~U_{ref} is loaded depending N;~~
~~stray capacitance of switches are charged or dis- every change;~~

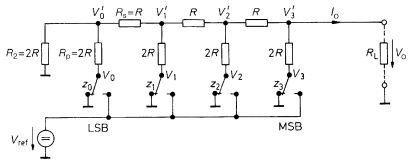
Ladder network



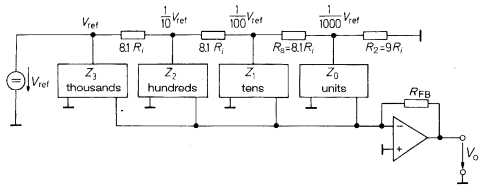
TIP:
~~difficult for manufacturing because of different R;~~
~~U_{ref} is loaded depending N;~~
~~strai capacitance of switches are charged or dis- every change;~~

$$U_{out} = -U_{ref}\frac{N}{N_{max}+1}$$

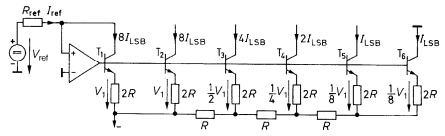
Ladder network converter without any amp



Decade Weighting Ladder network

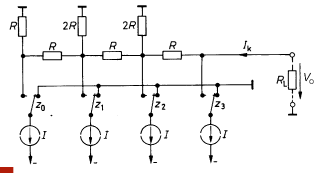


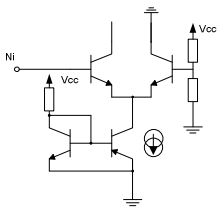
Current adding converter



TIP:
different currents of transistors - multiemiter transistors are required

Current switches with a ladder





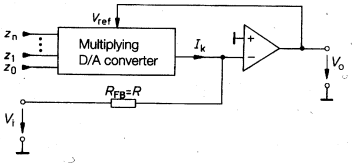
$$U_{out} = 2I\frac{N}{N_{max}+1}(2R \parallel R_L)$$

Multiplying converters

$$\left.\begin{aligned} u_{out} &= U_{ref}\frac{L}{2^n} \\ U_{ref} &= u_{in} \end{aligned}\right\} \Rightarrow u_{out} = u_{in} \bullet \frac{L}{2^n}$$

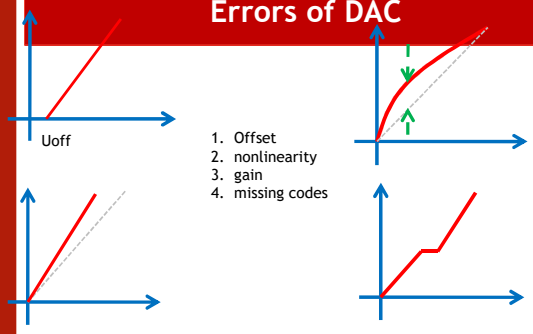
Every of till mentioned converters where multipying converters

Dividing converter



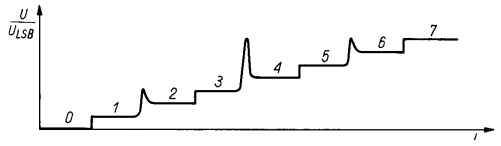
$$\left.\begin{aligned} U_{ref}\frac{N}{N_{max}+1} - U_{in} &= 0 \\ U_{ref} &= U_{out} \end{aligned}\right\} U_{out} = U_{in}\frac{N_{max}+1}{N} = \frac{U_{in}}{N}(N_{max}+1)$$

Errors of DAC



1. Offset
2. nonlinearity
3. gain
4. missing codes

Dynamic errors - glitch

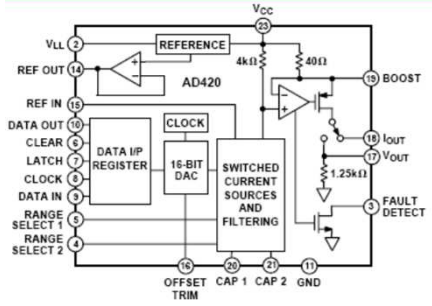


Converter AD420

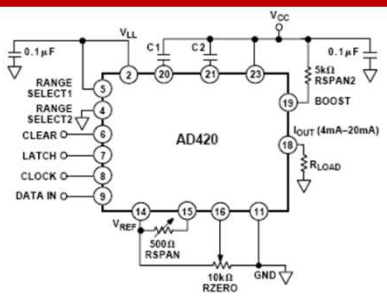
FEATURES

4 mA–20 mA, 0 mA–20 mA or 0 mA–24 mA Current Output
16-Bit Resolution and Monotonicity
±0.012% Max Integral Nonlinearity
±0.05% Max Offset (Trimmable)
±0.15% Max Total Output Error (Trimmable)
Flexible Serial Digital Interface (3.3 MBPS)
On-Chip Loop Fault Detection
On-Chip 5 V Reference (25 ppm/°C Max)
Asynchronous CLEAR Function
Maximum Power Supply Range of 32 V
Output Loop Compliance of 0 V to V_{CC} – 2.5 V
24-Lead SOIC and PDIP Packages

Converter AD420



ConverterAD420

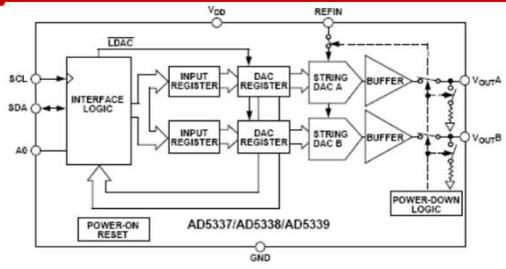


Converter AD5337,-8,-9

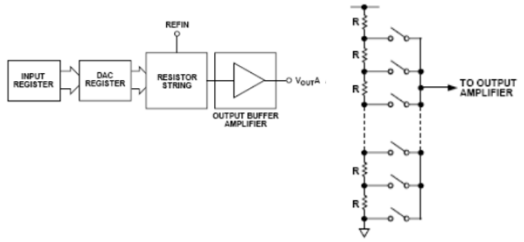
FEATURES

AD5337
2 buffered 8-bit DACs in 8-lead MSOP
AD5338, AD5338-1
2 buffered 10-bit DACs in 8-lead MSOP
AD5339
2 buffered 12-bit DACs in 8-lead MSOP
Low power operation: 250 mA @ 3 V, 300 mA @ 5 V
2-wire (I^2C compatible) serial interface
2.5 V to 5.5 V power supply
Guaranteed monotonic by design over all codes
Power-down to 80 nA @ 3 V, 200 nA @ 5 V
3 power-down modes
Double-buffered input logic
Output range: 0 V to V_{REF}
Power-on reset to 0 V
Simultaneous update of outputs ($\overline{LDAC}$ function)
Software clear facility
Data readback facility
On-chip rail-to-rail output buffer amplifiers
Temperature range: −40°C to +105°C

Converter AD5337,-8,-9



Converter AD5337,-8,-9



Converter AD5337,-8,-9

Parameter[1]	A Grade Min	A Grade Typ	A Grade Max	B Grade Min	B Grade Typ	B Grade Max	Unit	B Version[2] Conditions/Comments
DC PERFORMANCE[3, 4]								
AD5337								
Resolution		8			8		Bits	
Relative Accuracy		±0.15	±1		±0.15	±0.5	LSB	
Differential Nonlinearity		±0.02	±0.25		±0.02	±0.25	LSB	Guaranteed monotonic by design over all codes
AD5338								
Resolution		10			10		Bits	
Relative Accuracy		±0.5	±4		±0.5	±2	LSB	
Differential Nonlinearity		±0.05	±0.5		±0.05	±0.50	LSB	Guaranteed monotonic by design over all codes
AD5339								
Resolution		12			12		Bits	
Relative Accuracy		±2	±16		±2	±8	LSB	
Differential Nonlinearity		±0.2	±1		±0.2	±1	LSB	Guaranteed monotonic by design over all codes
Offset Error		±0.4	±3		±0.4	±3	% of FSR	
Gain Error		±0.15	±1		±0.15	±1	% of FSR	
Lower Deadband		20	60		20	60	mV	Lower deadband exists only if offset error is negative
Offset Error Drift[5]		−12			−12		ppm of FSR/°C	
Gain Error Drift[5]		−5			−5		ppm of FSR/°C	
Power Supply Rejection Ratio[3]		−60			−60		dB	$\Delta V_{DD} = \pm 10\%$
DC Crosstalk[5]		200			200		μV	$R_L = 2\ k\Omega$ to GND or V_{DD}

Converter ADV7129

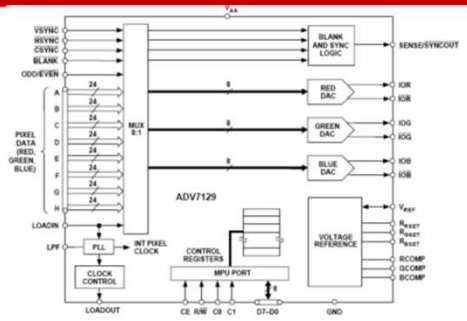
FEATURES

192-Bit Pixel Port Allows 2048 × 2048 × 24 Screen Resolution
360 MHz, 24-Bit True-Color Operation
Triple 8-Bit D/A Converters
8:1 Multiplexing
Onboard PLL
RS-343A/RS-170 Compatible Analog Outputs
TTL Compatible Digital Inputs
Internal Voltage Reference
Standard 8-Bit MPU I/O Interface
DAC-DAC Matching: Typ 2%, Adjustable to 0.02%
+5 V CMOS Monolithic Construction
304-Pin PQFP Package

APPLICATIONS

Ultrahigh Resolution Color Graphics
Image Processing
Drives 24-Bit Color 2K × 2K Monitors

Converter ADV7129



Summary

- Switches
- SH/TH circuits
- Resolution/sampling noise
- convertion principle
  - parallel
  - weighting
  - counting
- ladder network
- convertion errors (static and dynamic)

Test questions example:

- ~~What are the basic properties of switches ?~~
- ~~Enumerate types of electronic switches ?~~
- What is the difference between track&hold (TH) circuit and sample&hold (SH) ?
- What are the basic principles od DA converters ?
- What is the relationship between Channel Capacity and SNR/BW ?